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Characterization and Design of Millimeter-Wave Complementary Metal-Oxide-Semiconductor Components, and Broadband Low-Noise Amplifiers

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ABSTRACT OF THE
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This thesis focuses on the characterization and design of millimeter-wave CMOS components and broadband low-noise amplifiers. In the design of millimeter-wave circuits, accurate characterization of on-wafer active and passive components is of great importance. In this thesis, several well-known de-embedding techniques, which are used to characterize on-wafer devices, are reviewed, and their accuracies are investigated. A new de-embedding method for extracting the high frequency characteristics of a device-under-test is presented and applied to test structures manufactured in 28-nm CMOS technology. Excellent agreement is achieved between the simulated and experimental data up to 110 GHz, indicating that the proposed technique is an effective tool in characterization of mm-wave on-wafer components. Furthermore, design of active and passive components, which are used in the millimeter-wave low-noise amplifier circuit, is presented. Layout optimization techniques to improve the high frequency performances of these components are explained in detail. Simulation results are presented to demonstrate the performances of individual components. Finally, several issues concerning millimeter-wave low-noise amplifier design are discussed, such as stability, noise figure and different amplifier topologies. A three-stage full W-band low-noise amplifier achieving a flat gain of 15 dB and 5.5 dB noise figure over a very wideband is designed. Extensive simulation results showing the performance of the amplifier are presented.

Keywords: de-embedding, transmission line, millimeter-wave on-wafer CMOS components, MMIC, low-noise amplifier

Preface

The work for this thesis was carried out in the Department of Micro- and Nanosciences at Aalto University from May 2014 to May 2015.

I would like to thank my supervisor, Professor Kari Halonen, for giving me the opportunity to work on this thesis and for his valuable guidance. I would like to express my deep gratitude to my advisor, Dr. Mikko Varonen, for teaching, helping, guiding, motivating and inspiring me at every stage of my research.

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Denizhan Karaca

Contents

Symbols and abbreviations

Symbols

BW	bandwidth
C_d	shunt capacitance per unit length in distributed element model
C_{gd}	gate-to-drain capacitance
C_{gs}	gate-to-source capacitance
F	noise factor
f_{max}	maximum frequency of oscillation
f_t	unity current gain frequency
G	power gain
G_d	shunt conductance per unit length in distributed element model
g_{ds}	drain-to-source conductance
g_m	transconductance
$IP3$	third-order intercept point
K	stability factor
L_d	series inductance per unit length in distributed element model
NF_{min}	minimum noise figure
OCP_{1dB}	output 1-dB compression point
P_{dc}	power consumption
P_{sat}	saturated output power
Q_C	capacitive quality factor
Q_L	inductive quality factor
R_d	series resistance per unit length in distributed element model
R_g	gate resistance
R_s	source resistance
V_{ds}	drain to source voltage
V_{dd}	supply voltage
V_{gs}	gate to source voltage
Z_c	characteristic impedance
Z_{in}	input impedance
α	attenuation constant
β	phase constant
γ	propagation constant
ω	angular frequency
ϵ_0	vacuum permittivity
μ_0	vacuum permeability

Abbreviations

CMOS	complementary metal-oxide-semiconductor
CPW	co-planar waveguide
DC	direct current
DUT	device under test
EM	electromagnetic
GaAs	gallium arsenide
HFET	heterostructure field-effect transistor
InP	indium phosphide
LNA	low-noise amplifier
MAG	maximum available gain
MESFET	metal-semiconductor field effect transistors
MIM	metal-insulator-metal
MMIC	monolithic microwave integrated circuit
MOSFET	metal-oxide-semiconductor field effect transistors
MSG	maximum stable gain
NF	noise figure
RF	radio frequency
S-CPW	shielded co-planar waveguide

Figures and Tables

List of Figures

List of Tables

1 Introduction

1.1 CMOS Technology for Millimeter-Wave Applications

Millimeter-waves occupy the frequency spectrum from 30 GHz to 300 GHz, the region between the microwaves and terahertz waves, which corresponds to wavelengths from 10 millimeters down to 1 millimeter. Integrated circuits operating at mm-wave frequencies are called monolithic microwave integrated circuits (MMIC). These circuits typically perform functions such as power amplification, microwave mixing, low-noise amplification, and high-frequency switching which are required in wireless communication systems.

Traditionally, MMICs were mostly designed in III-V compound semiconductor technologies. Metal-semiconductor field effect transistors (MESFET), which are based on GaAS or InP technologies, and heterostructure field effect transistors (HFET) were preferred in MMIC design because of their high electron mobility, and consequently high speed. Silicon was not a competitor when it comes to mm-wave systems. However, this has changed in the past two decades. Thanks to the shrinking in the minimum feature size and pitch of photolithographic technologies, today CMOS technology offers transistors achieving very high f_t and f_{max} (>400 GHz) [1], and using very low power supplies. Moreover, minimum noise figure (NF_{min}) has been improved significantly for CMOS transistors. As a result, the last few years have witnessed an increasing interest in millimeter-wave communication systems and millimeter-wave applications of CMOS circuits. Mm-wave CMOS circuits have been an active research area with the applications in short distance high data rate communications [2], passive and active imaging systems [3]-[4] and broadband wireless networks [5]-[7].

One of the most important reasons of this high interest in utilizing CMOS for mm-wave applications is that it is low cost when produced in large volumes, mainly due to the worldwide manufacturing capacity of silicon technologies and its high yield. Although GaAs and InP technologies are still superior over CMOS in performance, they are costly for consumer electronics. Succeeding in the manufacture of low cost mm-wave devices with CMOS creates a huge market for consumer products. Active safety systems that feature adaptive cruise control and collision warning systems with automatic steering and breaking have become popular in recent years. Mm-wave circuits operating in 76-81 GHz band have been a good solution for such automotive radar applications [8]. Other good examples of mm-wave applications for consumer products are wireless transmission of high-definition video streams and wireless replacement of wired interconnections which are realized in 60 GHz spectrum.

It has been an important goal for circuit designers to build a whole communication system on the same chip in order to further bring down the manufacturing cost, complexity and to improve reliability. To this end, CMOS is a suitable tool since it is possible to build both digital and RF front-end circuits on silicon.

1.2 Motivation, Objective and Thesis Organization

As the CMOS technology scales down in the submicrometer range, total production cost increases mainly because of the rise in the mask cost. A mask set in 45-nm node can cost up to 2 million US dollars [9], and even more for newer technology nodes. Once the masks are produced, mass production of the circuits can be done with a little extra cost. Hence, it is crucial to get properly operating circuits on the first try which is possible only if the components are characterized accurately beforehand.

Due to the fact that CMOS technology mainly targets digital logic circuits, latest technology nodes are not always well established for mm-wave design when they are first released. In such cases, mm-wave characterization of passive devices is not complete, i.e. design kit models do not cover high frequency range (>20 GHz). The lack of accurate CMOS passive device models at mm-wave frequencies is a key barrier for designing complex CMOS transceiver circuits at these frequencies. Although the transistor models are usually valid up to 100 GHz, parasitic extraction tools might be unsatisfactory to account for geometry dependence of transistor characteristics in cases where the parasitic inductances, which are due to the via stacks and narrow metal lines connecting the transistor fingers, have a prominent effect on the transistor performance. Another issue is that even though the geometry of the oxide-metal stack of the technology is known to the designer, some critical material properties such as dielectric loss tangents and metal roughnesses inside the stack are not provided by the foundries. Moreover, dielectric materials in the oxide-metal stack are often dispersive, meaning that the material properties such as the relative permittivity and loss tangent of the dielectric layers are frequency dependent. Such changes in the material properties can, for example, alter the characteristic impedance of a transmission line, or the resonant frequency of a capacitor. Consequently, attempts to predict the actual behavior of the passive components at very high frequencies (>100 GHz) using electromagnetic field simulators might fail.

This thesis consists of two main parts. The first part aims to characterize high frequency behaviors of on-chip components in submicron CMOS technology nodes so that they can be utilized for mm-wave design. To this end, several de-embedding methods are analyzed and compared; their strengths and weaknesses are highlighted. A new de-embedding technique is proposed and proved to be accurate up to 110 GHz by measurements. On-wafer passive and active components, which were previously manufactured in 28-nm FDSOI CMOS technology, are characterized with the help of different de-embedding techniques. In the second part of the thesis, accuracy and efficiency of EM simulations in microstrip and co-planar waveguide environments are discussed. And finally, a full W-band low-noise amplifier (LNA) designed in microstrip environment is demonstrated. Design of active and passive devices utilized in the LNA circuit is explained in detail. The performances of the individual components and the overall circuit are demonstrated with extensive simulation results.

2 De-embedding Techniques

2.1 Introduction

At higher operating frequencies, circuits are more prone to non-ideal effects such as device parasitics and dielectric dispersion. To identify these non-idealities, high frequency measurements have to be done for individual active and passive components such as transistors and transmission lines. Conventional two port network parameters, impedance(Z-), admittance(Y-) , ABCD- parameters, are not appropriate for high frequency device characterization, because it is impractical and very challenging to realize open and short circuit terminations required to measure these data. However, scattering parameter (S-parameter) measurements exploit matched loads as terminations to define the network in terms of incident and reflected power waves, and therefore are suitable to characterize devices at high frequency. As all other types of measurements, S-parameter measurements are also performed at fixed bias. Therefore, when modeling active devices, measurement has to be carried out at several different bias points to characterize the small signal behavior of the device completely. All in all, S-parameter measurements stand to be the strongest tool for high frequency characterization. Throughout this thesis, Z, Y and ABCD two port parameters of the measured structures are used in several occasions, however it should be noted that they are always converted from S-parameters.

To be able to design fully functioning mm-wave integrated circuits, it is very important to characterize circuit components accurately. It is a fact that device models are only as accurate as the measurements that they are derived from. Because of this, extensive research has been done in the field of calibration and de-embedding for on-wafer measurements. Here, we will focus on the de-embedding issue.

The reason why a de-embedding process is required is that even after the measurement setup is calibrated up to the probe pads, test structures used to access the device under test (DUT) affect the measured characteristics. This effect of the test structure is significant due to the relatively large probe pads and the interconnections between the pads and DUT. For example, a MOSFET at the 28-nm node with a width of 20 μm has a very small gate-source capacitance of 5-15 fF that is comparable or less than the probe pad capacitance which can easily exceed 20 fF. In such a condition, measurement results would not reflect the actual characteristics of the MOSFET, and consequently, de-embedding would be needed.

There are mainly three classes of de-embedding techniques. The first group of techniques basically use lumped equivalent circuit models to de-embed the effect of the pads and the interconnects [10]-[21]. In general, three to five test structures are required to obtain accurate results with these methods. The second group of techniques utilizes cascade-based de-embedding techniques [22]-[28] which are based on calculating the transfer matrices of individual parasitic sources such as pads and interconnects and then removing their effect by matrix manipulations. For the methods in this group, usually three test structures are needed. The third class is a mixture of the first two. It assumes lumped equivalent circuits for the pads and interconnects, but also makes use of transfer matrices for the de-embedding purpose

[29]-[30]. Typically, two or three test structures are required for mixed methods.

2.2 Lumped Equivalent Circuit Model Based Techniques

2.2.1 Open-Short De-embedding

Open-short de-embedding is a simple, well known method introduced in [10]. Three test structures are required for the procedure; open, short and DUT. DUT structure is composed of probe pads, interconnects and transistor (Fig 2.2.1a). Open test structure is a duplicate of the DUT structure, with the device itself is removed (Fig 2.2.1b). In the short test structure, transistor is removed, then the signal and ground lines are shorted at the location of the transistor (Fig 2.2.1c). For the best results, the interconnects between the pads and DUT should be kept as short as possible.

In the open-short de-embedding method, it is assumed that all parallel parasitics are at the location of the pads. For this assumption to be valid, the interconnects between the pads and DUT should be kept relatively narrow.

The parasitics surrounding the transistor are shown in Figure 2.2.2a which represents the DUT structure equivalent circuit. Figures 2.2.2b and 2.2.2c represent the open and short test structures' equivalent circuits respectively. Transistor admittance parameters can be extracted as follows,

$$[Y_{DUT,os}] = (([Y_{meas}] - [Y_{open}])^{-1} - ([Y_{short]} - [Y_{open}])^{-1})^{-1} \tag{2.2.1}$$

where

$[Y_{DUT,os}]$ is the de-embedded admittance matrix of the device under test with open-short method,

$[Y_{meas}]$ is the measured admittance matrix of the device under test structure,

$[Y_{open}]$ and $[Y_{short}]$ are the measured admittance matrices of the open and short test structures respectively.

2.2.2 Short-Open De-embedding

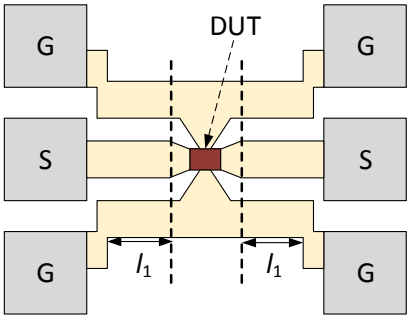
Short-open de-embedding is also a well known technique which uses the same test structures as in open-short de-embedding. In this method, the equivalent circuit shown in Figure 2.2.3a is assumed for the DUT structure, and the order of correction in open-short de-embedding is changed [11]. Figures 2.2.3b and 2.2.3c represent the equivalent circuits for the open and short structures respectively. The equation below gives the transistor admittance parameters.

$$[Y_{DUT,so}] = ([Y_{meas}]^{-1} - [Z_{short}])^{-1} - ([Y_{open}]^{-1} - [Z_{short}])^{-1} \tag{2.2.2}$$

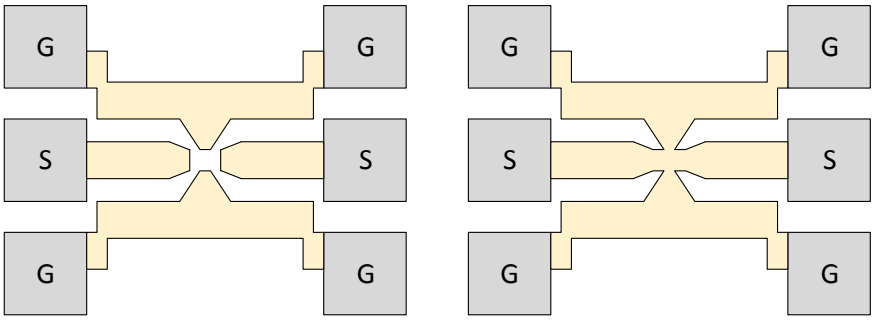
where

$[Y_{DUT,so}]$ is the de-embedded admittance matrix of the device under test with short-open method,

$[Z_{short}]$ is the measured impedance matrix of the short test structure respectively.



(a) DUT



(b) Open (c) Short

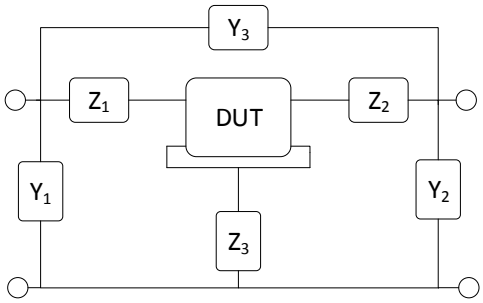
Figure 2.2.1: Layouts of the (a)DUT, (b)open and (c)short test structures

Despite the actual circuit includes parallel parasitics both at probe pads and near the device, parallel parasitics are assumed to be confined near the device. At first glance, it seems to be an incorrect assumption due to the fact that the major sources of the parallel capacitances are the probe pads. However, it was shown that the results from this method agree with open-short de-embedding up to 50 GHz [11].

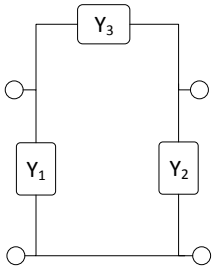
2.2.3 Pad-Short-Open De-embedding

To improve the open-short and short-open de-embedding techniques, a more comprehensive method was developed in [12]. In the previous methods, parallel parasitics are assumed to be located either at the location of the pads or near the device. In pads-short-open method, the effect of parallel parasitics is distributed over the probe pads and near the device.

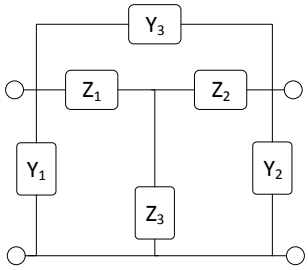
In addition to the test structures in the previously introduced methods, one extra test structure is required for this procedure which is composed of only the pads where interconnects and the DUT are removed(Fig 2.2.4). The equivalent circuit of the DUT structure is shown in Figure 2.2.5a. Figures 2.2.5b, 2.2.5c and 2.2.5d represent the equivalent circuits of the open, short and pads-only test structures, respectively.



(a) DUT



(b) Open



(c) Short

Figure 2.2.2: Lumped equivalent circuit models in open-short de-embedding

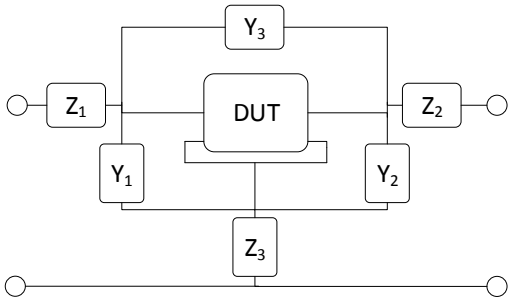
Admittance parameters of the transistor can be extracted as follows,

$$[Y_{DUT,pso}] = [Y_a] - [Y_b] \tag{2.2.3}$$

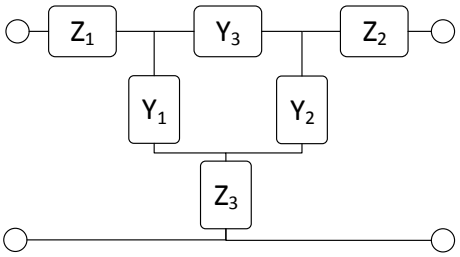
where
$[Y_a] = (([Y_{meas}] - [Y_{pad}])^{-1} - ([Y_{short}] - [Y_{pad}])^{-1})^{-1}$
$[Y_b] = (([Y_{open}] - [Y_{pad}])^{-1} - ([Y_{short}] - [Y_{pad}])^{-1})^{-1}$
$[Y_{DUT,pso}]$ is the de-embedded admittance matrix of the device under test with pad-short-open method,
$[Y_{pad}]$ is the measured admittance matrix of the pads-only test structure respectively.

2.2.4 Three Step De-embedding

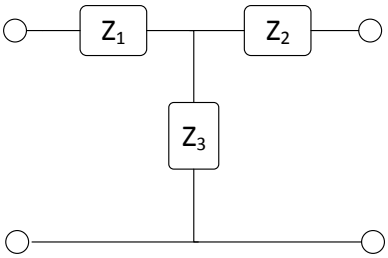
A more complicated method was proposed in [13]. In addition to the DUT and open test structures shown in Figures 2.2.1a and 2.2.1b, three extra on-wafer test structures , $short_1$, $short_2$ and $thru$, are required. Figure 2.2.6 illustrates these test structures. Equivalent circuits for the test structures are shown in Figure 2.2.7. The admittances Y_1 and Y_2 represent the shunt parasitics due to the probe pads, while Y_3 models the coupling between the input and output ports of the DUT. Z_1 and Z_2 represent the series parasitics originating from the interconnects. Z_3 models the ground leads toward the DUT.



(a) DUT



(b) Open



(c) Short

Figure 2.2.3: Equivalent circuit models in short-open de-embedding, and in the new de-embedding method

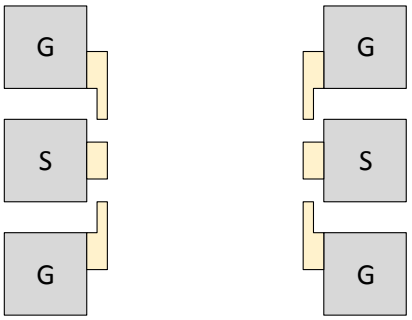


Figure 2.2.4: Pads-only test structure

Values of these parasitic components are given by,

$$Y_1 = Y_{open,11} + Y_{open,12} \tag{2.2.4}$$

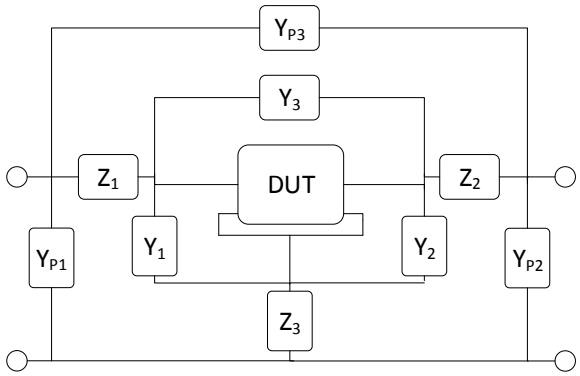
$$Y_2 = Y_{open,22} + Y_{open,12} \tag{2.2.5}$$

$$Y_3 = (\frac{1}{Y_{thru,12}} - \frac{1}{Y_{open,12}})^{-1} \tag{2.2.6}$$

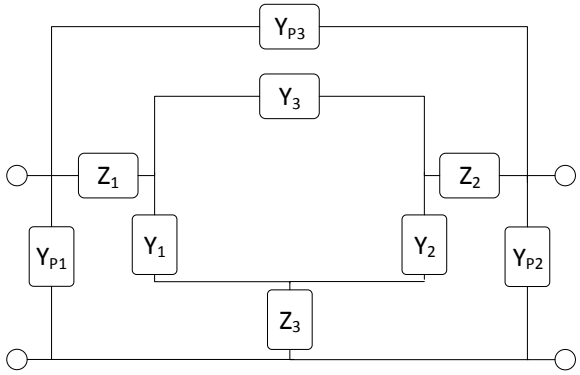
$$Z_1 = \frac{1}{2}(\frac{-1}{Y_{thru,12}} + \frac{1}{Y_{sh1,11} - Y_1} - \frac{1}{Y_{sh2,22} - Y_2}) \tag{2.2.7}$$

$$Z_2 = \frac{1}{2}(\frac{-1}{Y_{thru,12}} - \frac{1}{Y_{sh1,11} - Y_1} + \frac{1}{Y_{sh2,22} - Y_2}) \tag{2.2.8}$$

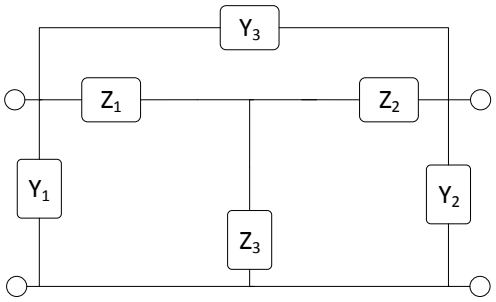
$$Z_3 = \frac{1}{2}(\frac{1}{Y_{thru,12}} + \frac{1}{Y_{sh1,11} - Y_1} + \frac{1}{Y_{sh2,22} - Y_2}) \tag{2.2.9}$$



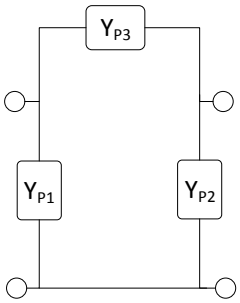
(a) DUT



(b) Open



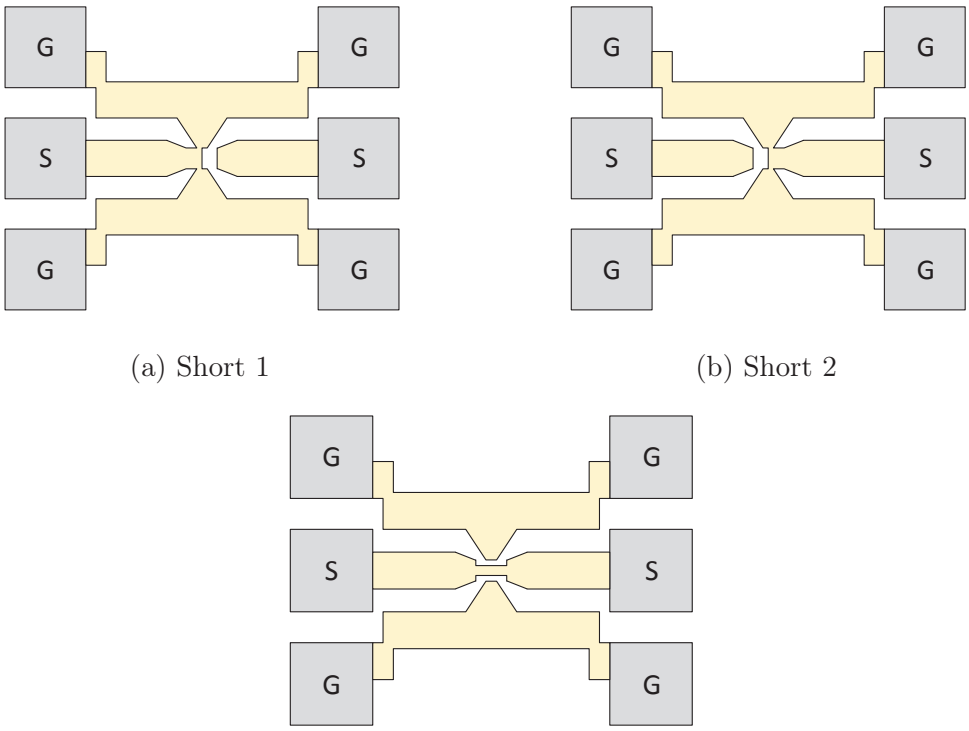
(c) Short



(d) Pads-only

Figure 2.2.5: Equivalent circuit models in pads-short-open de-embedding

where
Y_{thru} is the admittance matrix of the thru test structure,
Y_{sh1} is the admittance matrix of the short 1 test structure,
Y_{sh2} is the admittance matrix of the short 2 test structure respectively.



(a) Short 1

(b) Short 2

(c) Thru

Figure 2.2.6: Test structures used in the three step de-embedding method

Knowing the values of parasitic components, one can de-embed the two-port network parameters of the DUT as follows,

$$[Y_A] = [Y_{meas}] - \begin{bmatrix} Y_1 & 0 \\ 0 & Y_2 \end{bmatrix} \tag{2.2.10}$$

Admittance matrix $[Y_A]$ is converted to impedance matrix $[Z_A]$,

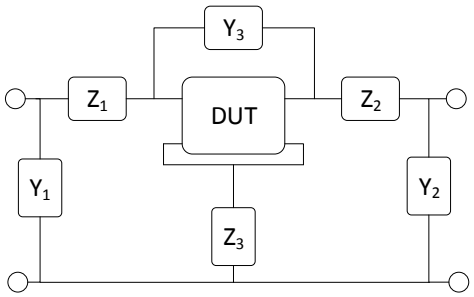
$$[Z_B] = [Z_A] - \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix} \tag{2.2.11}$$

Impedance matrix $[Z_B]$ is converted to admittance matrix $[Y_B]$,

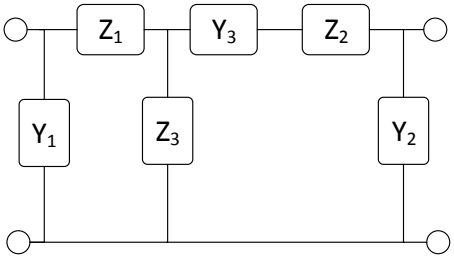
$$[Y_{DUT,three}] = [Y_B] - \begin{bmatrix} Y_3 & -Y_3 \\ -Y_3 & Y_3 \end{bmatrix} \tag{2.2.12}$$

where

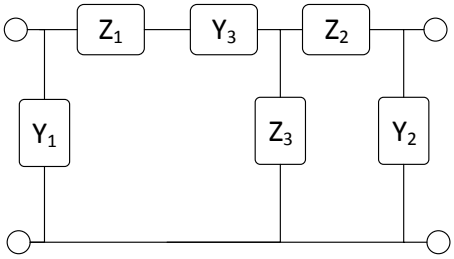
$[Y_{DUT,three}]$ is the de-embedded admittance matrix of the device under test with the three-step de-embedding method.



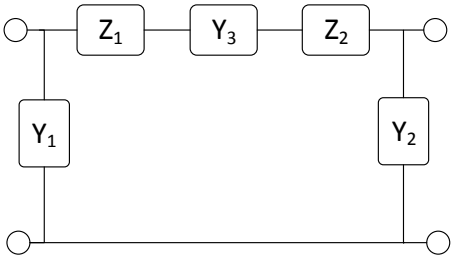
(a) DUT



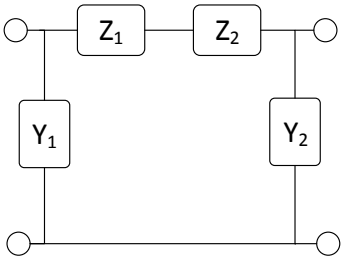
(b) Short 1



(c) Short 2



(d) Open



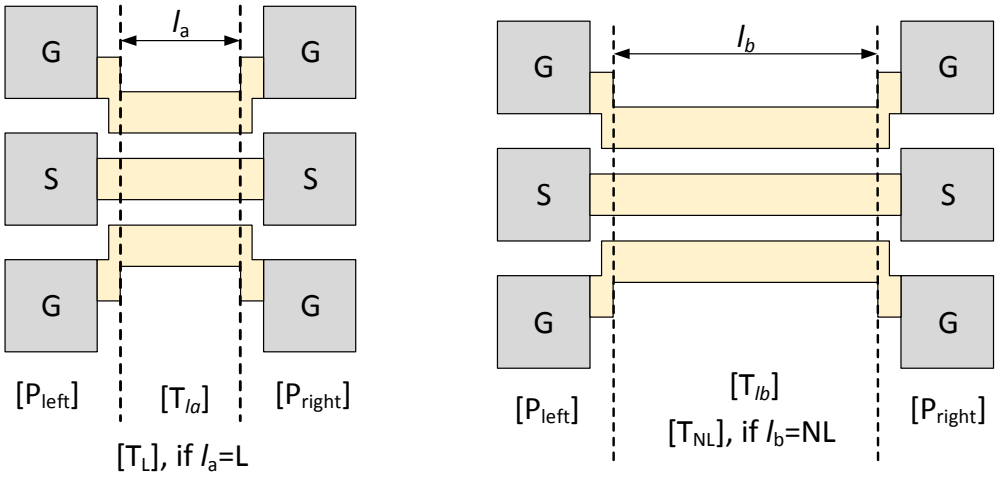
(e) Thru

Figure 2.2.7: Equivalent circuit models in three-step de-embedding

2.3 Cascade-Based Techniques

2.3.1 L-NL Method

In this method two line sections of lengths L and NL (N is an integer higher than one) with attached pads are used to characterize the transmission line [22]. The transmission line test structures are decoupled into a series cascade of three two port networks which are the left-side pad, line and right-side pad. Figures 2.3.1a and 2.3.1b illustrate the test structures and the decoupling of the networks.



(a) Short Line

(b) Long Line

Figure 2.3.1: Test Structures used in L-NL and Alain's methods

Multiplication sum of ABCD matrices $[P_{left}]$ and $[P_{right}]$ can be extracted using the following equations:

$$[T_{LM}] = [P_{left}] \cdot [T_L] \cdot [P_{right}] \tag{2.3.1}$$

$$[T_{NLM}] = [P_{left}] \cdot [T_{NL}] \cdot [P_{right}] = [P_{left}] \cdot [T_L]^N \cdot [P_{right}] \tag{2.3.2}$$

$$[P_{left}] \cdot [P_{right}] = ([T_{NLM}] \cdot [T_{LM}]^{-1})^{1/(1-N)} \cdot [T_{LM}] \tag{2.3.3}$$

where

$[T_{LM}]$ and $[T_{LM}]$	are the measured (uncorrected) ABCD parameters of the L and NL long interconnects,
$[T_L]$ and $[T_{NL}]$	are the ABCD parameters of the L and NL long interconnects without the probe pads,
$[P_{left}]$ and $[P_{right}]$	are the ABCD parameters of the left and right pads, respectively.

Left and right pads are exactly the same except that one of them is mirrored around vertical axis. An equivalent circuit shown in Figure 2.3.2 is assumed and the multiplication of ABCD matrices $[P_{left}]$ and $[P_{right}]$ is used to derive the two-port parameters of the pad as follows:

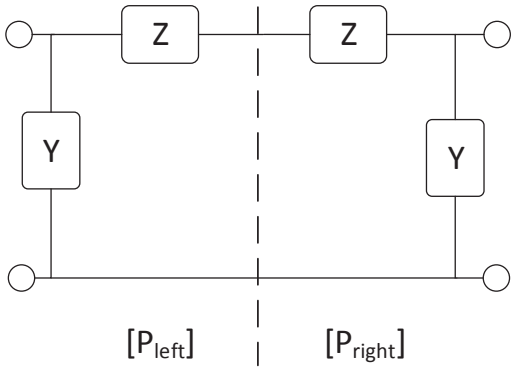


Figure 2.3.2: Assumed pad model

$$\begin{aligned}[P_{left}] \cdot [P_{right}] &= \begin{bmatrix} 1 & Z \\ Y & 1+YZ \end{bmatrix} \cdot \begin{bmatrix} 1+YZ & Z \\ Y & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1+2YZ & 2Z \\ 2Y(YZ+1) & 1+2YZ \end{bmatrix} = \begin{bmatrix} A_{LR} & B_{LR} \\ C_{LR} & D_{LR} \end{bmatrix} \end{aligned} \tag{2.3.4}$$

and therefore,

$$Z = \frac{B_{LR}}{2} \quad , \quad Y = \frac{C_{LR}}{1+A_{LR}} = \frac{C_{LR}}{1+D_{LR}} \tag{2.3.5}$$

After extracting $[P_{left}]$ and $[P_{right}]$, two port parameters of the line sections can be obtained as follows:

$$[T_L] = [P_{left}]^{-1} \cdot [T_{LM}] \cdot [P_{right}]^{-1} \tag{2.3.6}$$

$$[T_{NL}] = [P_{left}]^{-1} \cdot [T_{NLM}] \cdot [P_{right}]^{-1} \tag{2.3.7}$$

The next step is calculating the transmission line parameters. To this end, formulas in [33] are used:

$$[T_L] = \begin{bmatrix} \cosh(\gamma L) & Z_c \sinh(\gamma L) \\ Z_c^{-1} \sinh(\gamma L) & \cosh(\gamma L) \end{bmatrix} = \begin{bmatrix} A_{T_L} & B_{T_L} \\ C_{T_L} & D_{T_L} \end{bmatrix} \tag{2.3.8}$$

$$Z_c = \sqrt{\frac{B_{T_L}}{C_{T_L}}} \ [\Omega] \tag{2.3.9}$$

$$\gamma = \frac{\cosh^{-1} A_{T_L}}{L} \tag{2.3.10}$$

where Z_c is the characteristic impedance and γ is the complex propagation constant of the line.

Once Z_c and γ are determined, one can calculate the distributed line parameters from the standard transmission line relationships:

$$\gamma = \sqrt{(R_d + jwL_d)(G_d + jwC_d)} = \alpha + j\beta \tag{2.3.11}$$

$$Z_c = \sqrt{\frac{(R_d + jwL_d)}{(G_d + jwC_d)}} \tag{2.3.12}$$

$$R_d = Re(\gamma Z_c) \ , \ L_d = \frac{Im(\gamma Z_c)}{w} \ , \ G_d = Re(\gamma / Z_c) \ , \ C_d = \frac{Im(\gamma / Z_c)}{w} \tag{2.3.13}$$

where
R_d is the series resistance per unit length, in Ω/m.
L_d is the series inductance per unit length, in H/m.
G_d is the shunt conductance per unit length, in S/m.
C_d is the shunt capacitance per unit length, in F/m.

In [22], the procedure is limited to characterizing the transmission line and the pads. In this study, the idea is carried a step further and used to characterize a device under test. For this purpose, a DUT structure as in Figure 2.2.1a is required in addition to the two line sections of lengths L and NL. It is not practical to use long line sections in DUT structure (length l_1 in Figure 2.2.1a) since it will occupy a large area on the chip. However, if l_1 is chosen to be equal to L (or N·L), which is usually relatively long, two port parameters of the DUT can be extracted by further manipulation of ABCD matrices of the test structures, pads and lines as follows,

$$[T_{DUT,L-NL}] = [T_L]^{-1} \cdot [P_{left}]^{-1} \cdot [T_{meas}] \cdot [P_{right}]^{-1} \cdot [T_L]^{-1} \tag{2.3.14}$$

where
$[T_{DUT,L-NL}]$ is the de-embedded ABCD matrix of the device under test with the L-NL method,
$[T_{meas}]$ is the measured ABCD matrix of the device under test structure, respectively.

If l_1 is chosen to be a shorter line section than L to save area on the chip, a different kind of approach, where a length scalable transmission line model is utilized, can be followed. In [31], it is shown that the ADS two-port transmission line model (TLINP) can be used as an effective tool in modeling of transmission lines at mm-wave frequencies. The parameters of the TLINP model are tabulated in Table 1.

Table 1: ADS practical transmission line model parameters

Model Parameter	**Description**	**Units**
Z	Characteristic impedance	Ohm
L	Physical length	μm
K	Effective dielectric constant	None
A	Attenuation	dB/meter
F	Frequency for scaling attenuation	GHz
TanD	Dielectric loss tangent	None

Parameter A specifies the conductor loss only, and the dielectric loss is specified by TanD. Although the characteristic impedance parameter Z has to be real, due

to the reason that conductor and dielectric losses can be specified separately, the component is not assumed to be distortionless. Therefore, the actual characteristic impedance of the line may be complex and frequency dependent. There are two possible ways of extracting the required model parameters. The first way is using the calculated transmission line parameters under the assumption of low loss as follows:

$$Z_c = \sqrt{\frac{L_d}{C_d}} \ , \ A = 8.686\frac{R_d}{2Z_c} \ , \ TanD = \frac{G_d}{wC_d} \ , \ K = \frac{L_d C_d}{\epsilon_0 \mu_0} \tag{2.3.15}$$

Second and probably the better approach is using the optimization tool of ADS in order to fit the simulated model S-parameters to the extracted S-parameters. For this purpose, first, ABCD matrices $[T_L]$ and $[T_{NL}]$ are converted to S-parameters to be compared with the simulated TLINP model S-parameters. Then, the length in the TLINP model is set to the actual line section length (L or NL) and the rest of the parameters are left variable during the optimization process. It is a good idea to compare the results from the optimization approach with the calculated values from the former approach, in case the optimization tool gives a non-physical solution which give the same overall response. Moreover, to prevent optimization tool from giving such results, one can set the initial values of the parameters to the calculated values from the former method and give a $\pm 20\%$ range to all parameters (except obviously the length parameter) for optimization.

Once the parameters for the ADS transmission line model are found, the rest of the procedure is straightforward. First, ABCD matrix of a TLINP component, having the extracted model parameters and a length of l_1, is calculated in ADS. Then similar ABCD matrix manipulations are done as in equation 2.3.14,

$$[T_{DUT,L-NL}] = [T_{l_1}]^{-1} \cdot [P_{left}]^{-1}[T_{meas}] \cdot [P_{right}]^{-1} \cdot [T_{l_1}]^{-1} \tag{2.3.16}$$

where
$[T_{l_1}]$ is the ABCD matrix of a line of length l_1.

Special Case: L-2L
If the length of the longer line is chosen to be twice of that of the shorter line, equation 2.3.3 can be further simplified into the following form [23],

$$[P_{left}] \cdot [P_{right}] = ([T_{LM}]^{-1} \cdot [T_{2LM}] \cdot [T_{LM}]^{-1})^{-1} \tag{2.3.17}$$

where $[T_{2LM}]$ is the measured ABCD parameters of the 2L long line

2.3.2 Alain's Method

A similar approach to the L-NL method was proposed in [24] which requires two line sections in order to characterize the transmission line. The superiority of this method over L-NL method is that the line lengths do not have to be in the form of L and NL. Two line sections of arbitrary lengths l_a and l_b, where $l_b > l_a$, with attached pads are required to employ this method. And by choosing $l_b < 2l_a$ it is possible to save silicon area. The transmission line test structures are decoupled into a series

cascade of three two port networks which are the left-side pad, line, and right-side pad. Figures 2.3.1a and 2.3.1b illustrate the test structures and the decoupling of the networks. The extraction procedure is as follows:

$$\begin{aligned} [T_{Ml_a}] &= [P_{left}] \cdot [T_{l_a}] \cdot [P_{right}] \\ [T_{Ml_b}] &= [P_{left}] \cdot [T_{l_b}] \cdot [P_{right}] \end{aligned} \tag{2.3.18}$$

$$\begin{aligned} [T^h_{l_b-l_a}] &= [T_{l_b}] \cdot [T_{l_a}]^{-1} \\ &= [P_{left}] \cdot [T_{l_b}] \cdot [T_{l_a}]^{-1} \cdot [P_{left}]^{-1} \\ &= [P_{left}] \cdot [T_{l_b-l_a}] \cdot [P_{left}]^{-1} \end{aligned} \tag{2.3.19}$$

where

$[T_{l_a}]$ and $[T_{l_b}]$ are the measured ABCD parameters of the l_a and l_b long interconnects,

$[T_{l_b-l_a}]$ is the ABCD parameters of a l_a-l_b long interconnect respectively.

With the assumption that pads can be modeled only by a lumped admittance Y_L, one can write

$$[P_{left}] = [P_{right}] = \begin{bmatrix} 1 & 0 \\ Y_L & 1 \end{bmatrix} \tag{2.3.20}$$

$$[T^h_{l_b-l_a}] = \begin{bmatrix} 1 & 0 \\ Y_L & 1 \end{bmatrix} \cdot [T_{l_b-l_a}] \cdot \begin{bmatrix} 1 & 0 \\ -Y_L & 1 \end{bmatrix} \tag{2.3.21}$$

Above equation is equivalent to a cascade system of a pad with admittance Y_L, a line section with length $l_a - l_b$ and a pad with admittance $-Y_L$. Then, using admittance parameter properties one can write

$$[Y^h_{l_b-l_a}] = [Y_{l_b-l_a}] + \begin{bmatrix} Y_L & 0 \\ 0 & -Y_L \end{bmatrix} \tag{2.3.22}$$

Then Y parameters of the $l_a - l_b$ long line section can be written as follows,

$$[Y_{l_b-l_a}] = \frac{[Y^h_{l_b-l_a}] + Swap([Y^h_{l_b-l_a}])}{2} \tag{2.3.23}$$

where Swap(Y) swaps the ports 1 and 2 of a two port:

$$Swap(\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}) = \begin{bmatrix} a_{22} & a_{21} \\ a_{12} & a_{11} \end{bmatrix} \tag{2.3.24}$$

After the Y matrix for the line section is obtained, it is converted into ABCD matrix and the equations 2.3.8 to 2.3.13 are used to extract the transmission line parameters. From this point on, knowing the pad and line characteristics, same procedure explained in section 2.3.1 can be used to extract the DUT characteristics.

The inferior part of Alain's method is that the probe pad is assumed to behave as a shunt admittance only, whereas in L-NL method it is a combination of a shunt admittance and a series impedance which is a more complete and accurate model. Especially if the pads are not designed carefully, such that the discontinuity between the pad and the line is short and smooth (or tapered if necessary), the discontinuity can have a considerable effect at high frequencies.

2.3.3 Open-Short Pads Method

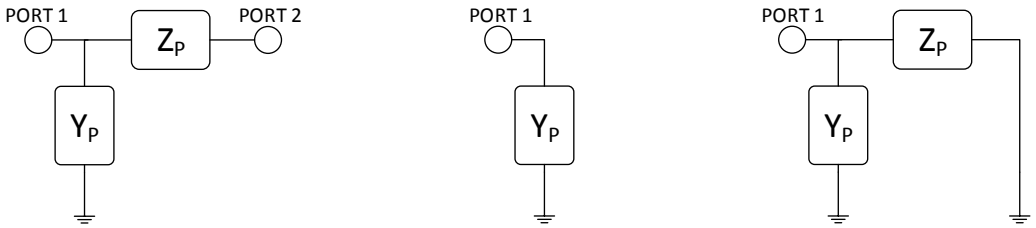
So far, matrix manipulations have been employed to extract the pad characteristics using the transmission line test structure measurements. Another way to characterize the pad is using the open and short pad measurements [31]. Figures 2.3.3a and 2.3.3b represent a possible way of realizing open and short ground-signal-ground (GSG) pad structures, respectively. Four test structures (open pad, short pad, DUT

(a) Open Pad (b) Short Pad

Figure 2.3.3: Open-short pad test structures

structure and line structure with attached pads) are required in total. However the total size of the open and short pads is considerably smaller than the size of a second line structure which is used in L-NL and Alain's methods.

Similar to the previous approaches, a pad model composed of a shunt admittance and a series impedance is assumed for the pad in this method. The equivalent circuit model for the whole pad, open and short pads are shown in Figures 2.3.4a, 2.3.4b and 2.3.4c, respectively. One port measurements of open and short structures are used to derive the two port network parameters of the pad.



(a) Whole pad (b) Open (c) Short

Figure 2.3.4: Equivalent circuit models of the pad

Calculation of Y_P, Z_P and ABCD matrix of the pad is as follows:

$$Y_P = Y_{pad,open} \tag{2.3.25}$$

$$Z_P = \frac{1}{Y_{pad,short} - Y_P} \tag{2.3.26}$$

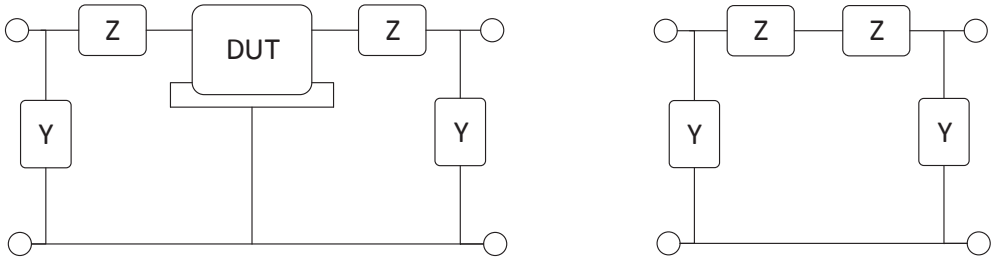
$$[T_{pad}] = \begin{bmatrix} 1 & Z_P \\ Y_P & 1 + Y_P Z_P \end{bmatrix} \tag{2.3.27}$$

where $Y_{pad,open}$ and $Y_{pad,short}$ are the measured admittance parameters of the open and short pad structures, $[T_{pad}]$ is the ABCD matrix of the probe pad respectively. Knowing the ABCD parameters of the pad, one can obtain the transmission line parameters and 2 port parameters of the DUT as explained in section 2.3.3, where $[T_{pad}]$ corresponds to $[P_{left}]$.

2.4 Mixed Techniques

2.4.1 Thru-only De-embedding

Thru-only de-embedding proposed in [29] is one of the simplest methods accounting for test structure parasitics. It makes use of a thru test structure (Fig 2.2.6c) to remove the shunt and series parasitic contributions caused by pads and interconnects in the DUT structure. Assumed equivalent models of the DUT and thru test structures are shown in Figure 2.4.1. Y and Z components represent shunt and series parasitics



(a) DUT (b) Thru

Figure 2.4.1: Equivalent circuit models of the test structures in thru-only de-embedding method

caused by pads and interconnects, respectively. They can be calculated as follows:

$$Y = Y_{thru,11} + Y_{thru,12} \tag{2.4.1}$$

$$Z = -(1/2Y_{thru,12}) \tag{2.4.2}$$

where Y_{thru} is the measured admittance parameters of the thru structure.

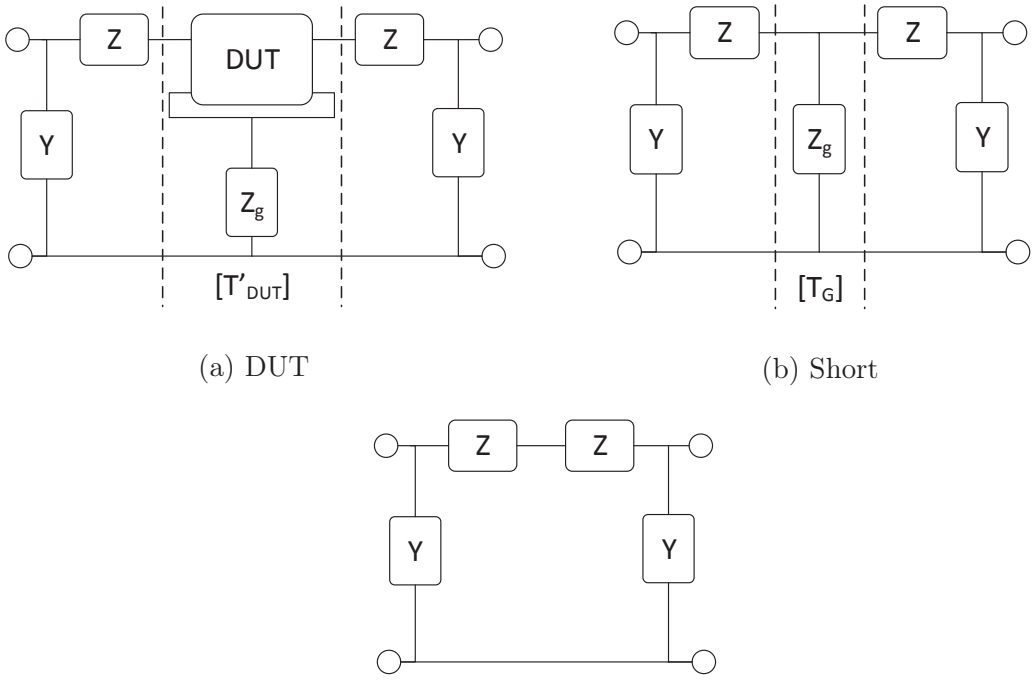
Next, ABCD matrix manipulations are done in order to get the 2 port parameters of the DUT:

$$[T_{DUT,thru}] = \begin{bmatrix} 1 & Z \\ Y & 1 + YZ \end{bmatrix}^{-1} \cdot [T_{meas}] \cdot \begin{bmatrix} 1 + YZ & Z \\ Y & 1 \end{bmatrix}^{-1} \tag{2.4.3}$$

where
$[T_{DUT,thru}]$ is the de-embedded ABCD matrix of the device under test with the thru-only method.

2.4.2 Thru-Short De-embedding

An improved version of thru-only de-embedding was proposed in [30] at the expense of an extra short test structure. The superiority of this method over the thru-only method is that it accounts for the parasitics caused by the ground leads towards the DUT. The equivalent circuit is shown in Figure 2.4.2. Values of Y and Z are



(a) DUT

(b) Short

(c) Thru

Figure 2.4.2: Equivalent circuit models of the test structures in the thru-short de-embedding method

calculated using formulas 2.4.1 and 2.4.2. Two port parameters of the DUT can be found as follows,

$$\begin{aligned}[T'_{DUT}] &= \begin{bmatrix} 1 & Z \\ Y & 1+YZ \end{bmatrix}^{-1} \cdot [T_{meas}] \cdot \begin{bmatrix} 1+YZ & Z \\ Y & 1 \end{bmatrix}^{-1} \\ [T_G] &= \begin{bmatrix} 1 & Z \\ Y & 1+YZ \end{bmatrix}^{-1} \cdot [T_{short}] \cdot \begin{bmatrix} 1+YZ & Z \\ Y & 1 \end{bmatrix}^{-1} \end{aligned} \tag{2.4.4}$$

ABCD matrices $[T'_{DUT}]$ and $[T_G]$ are converted to impedance matrices $[Z'_{DUT}]$ and $[Z_G]$. Then,

$$[Z_{DUT,thrus}] = [Z'_{DUT}] - [Z_G] \tag{2.4.5}$$

where
$[Z_{DUT,thrus}]$ is the de-embedded impedance matrix of the device under test with the thru-short method.

2.5 New De-embedding Technique for the DUT and DUT Access Characterization

2.5.1 Effect of the DUT Access

The access required to connect the DUT to the transmission lines can have a noteworthy effect on the device performance, as it creates additional parasitics due to via stacks and the coupling between different sections of access metals. This effect can be critical, especially in co-planar wave guide (CPW) environment where the DUT access is a physically large structure due to the long ground legs as shown in Figure 2.5.1.

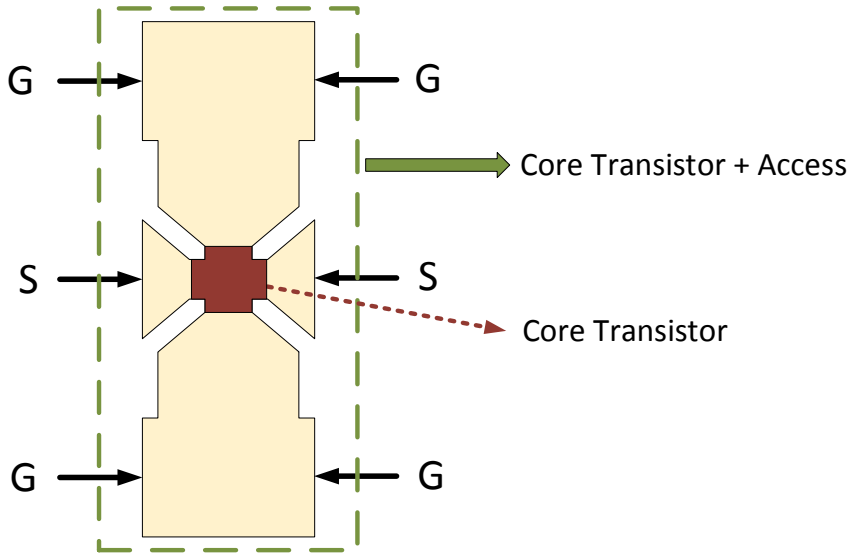


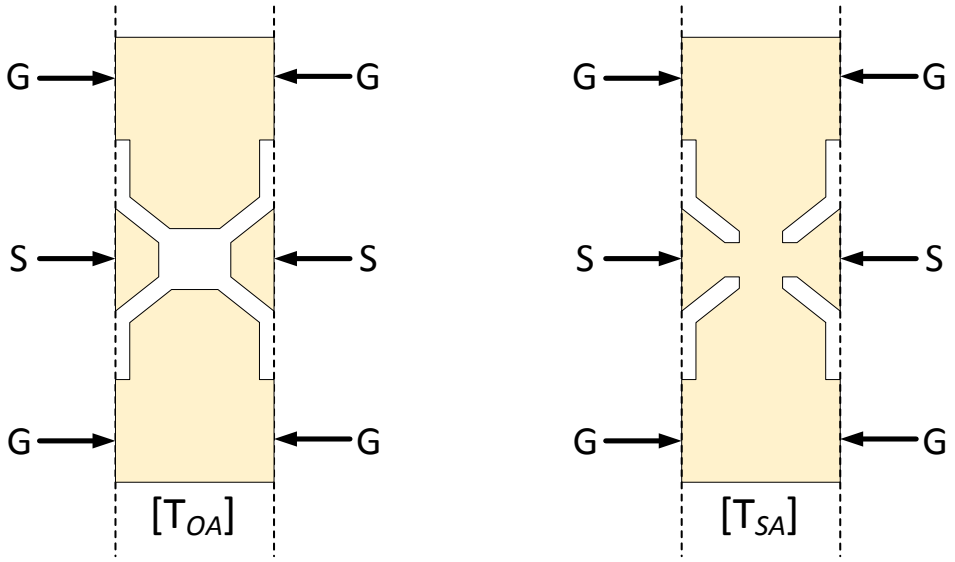
Figure 2.5.1: DUT access structure

In lumped equivalent circuit model based and mixed de-embedding techniques, the effect of the access is de-embedded, while in cascade-based techniques it is included in the resultant DUT characteristic. Therefore, there are mainly two options to account for the access parasitics in a circuit design process:

Option 1: Employ a cascade-based technique and use the resultant DUT characteristics, which includes the parasitics from access, in the design.

Option 2: Characterize the core transistor and access separately, use the combination of them in the design.

Considering that the transistors have to be used along with the access all the time, one may prefer *Option 1* since it is simpler. However, characterizing the access has two main advantages over the former method. First, in mature CMOS technology



(a) Open (b) Short

Figure 2.5.2: Open and short access structures

nodes, post layout design kit models for the transistors are proved to be valid for very high frequencies (up to 100 GHz or higher) which is also the case for the latest 28-nm node as will be shown in this thesis in section 3. However, generally, inductive parasitic effect of the transistor access can not be included in the post layout design kit models. EM simulations can be carried out to overcome this problem, however in [32], it is shown that EM simulations can also fail to model the access accurately. Therefore, if transistors with different widths are to be used in the design, several DUT structures are required to extract the access included characteristics of each transistor in case of the use of *Option 1*. On the contrary, one can characterize the access, which is usually the same structure for different sized transistors, and use it for transistors of different sizes by combining it with the design kit models. Second, if a brand new CMOS technology node is to be used for the design, it is usually a good idea to test how accurate the design kit model is at very high frequencies. To this end, one has to extract the core transistor characteristic and compare it with the design kit model.

Unfortunately, the currently existing de-embedding techniques either do not take the effect of DUT access into account or they do take it into account but do not characterize it after subtracting its effect from the measurement. Therefore, in this section, a new method to characterize both DUT and DUT access is proposed [34].

2.5.2 Theory of the New De-embedding Technique

The new technique makes use of previously introduced de-embedding methods to model the pads and the interconnects, then extracts the DUT and DUT access with few additional steps. The procedure can be summarized in the following four steps: 1) Extract the ABCD matrices of the pads and the interconnects using one of the

methods explained in section 2.3.
2) Extract the ABCD matrices of open and short access structures shown in Figure 2.5.2 as follows,

$$[T_{OA}] = [T_{line}]^{-1} \cdot [P_{left}]^{-1} \cdot [T_{open}] \cdot [P_{right}]^{-1} \cdot [T_{line}]^{-1} \tag{2.5.1a}$$
$$[T_{SA}] = [T_{line}]^{-1} \cdot [P_{left}]^{-1} \cdot [T_{short}] \cdot [P_{right}]^{-1} \cdot [T_{line}]^{-1} \tag{2.5.1b}$$

where
$[T_{OA}]$ and $[T_{SA}]$ are the ABCD matrices of the open and short access structures,
$[T_{open}]$ and $[T_{short}]$ are the measured ABCD matrices of the open and short test structures,
$[T_{line}]$ is the ABCD matrix of the line section connecting the pads and the access respectively.

3) Convert ABCD matrices $[T_{OA}]$ and $[T_{SA}]$ to $[Z_{OA}]$ and $[Z_{SA}]$ which are the impedance matrices of open and short accesses respectively.
4) Assume the equivalent circuit models introduced in section 2.2.2 Figure 2.2.3 for the open, short and DUT connected access structures, and extract the parasitic components as follows:

$$[Y_{inner}] = ([Z_{OA}] - [Z_{SA}])^{-1} \tag{2.5.2a}$$
$$Z_1 = Z_{SA,11} - Z_{SA,12} \tag{2.5.2b}$$
$$Z_2 = Z_{SA,22} - Z_{SA,12} \tag{2.5.2c}$$
$$Z_3 = Z_{SA,12} \tag{2.5.2d}$$
$$Y_1 = Y_{inner,11} + Y_{inner,12} \tag{2.5.2e}$$
$$Y_2 = Y_{inner,22} + Y_{inner,12} \tag{2.5.2f}$$
$$Y_3 = -Y_{inner,12} \tag{2.5.2g}$$

Once Z_1, Z_2, Z_3, Y_1, Y_2 and Y_3 are calculated, they can be combined with transistors of different sizes in the circuit simulators to account for the access parasitics, as long as the transistor layout size is small enough that it can fit the area left open in the open test structure.

Two-port parameters of the core DUT are obtained by performing two additional steps:
1) Extract two port parameters of the access included transistor.

$$[T_{DUT+access}] = [T_{line}]^{-1} \cdot [P_{left}]^{-1} \cdot [T_{meas}] \cdot [P_{right}]^{-1} \cdot [T_{line}]^{-1} \tag{2.5.3}$$

2) Convert ABCD matrix $[T_{DUT+access}]$ to impedance matrix $[Z_{DUT+access}]$. Then use $[Z_{DUT+access}]$, $[Z_{OA}]$ and $[Z_{SA}]$ to extract the core transistor two port admittance parameters using a similar approach to the one in [11]:

$$[Y_{DUT,new}] = ([Z_{DUT+access}] - [Z_{SA}])^{-1} - ([Z_{OA}] - [Z_{SA}])^{-1} \tag{2.5.4}$$

where
$[Y_{DUT,new}]$ is the de-embedded admittance matrix of the core DUT with the new method.

2.6 Accuracy Investigation of De-embedding Methods

In this section, accuracies of the previously introduced de-embedding methods are examined. In order to imitate the test structure measurements, several circuit simulations were carried out in ADS, using pre-defined transistor, pad, line and access models which are summarized in Table 2.

Pad models presented in Table 2 are based on [12]. Distributed capacitive effect associated with the pads are represented by two lumped capacitance and one resistance (C_{P1},C_{P2} and R_{P1}). Resistance R_{P2} models the coupling between signal and ground pads through the substrate. L_{P1}, L_{P2}, R_{P3} and R_{P4} model the discontinuity between the pads and the transmission line. Access model shown in Table 2 accounts for the parasitic capacitances between the signal and ground legs of the access, and for the series inductive effect of each leg.

S-parameter simulation results of the test structure circuits are used in the formulas given in sections 2.2, 2.3 and 2.4 to extract the transistor model. Then, in order to test the accuracy of a de-embedding method, the weighted difference between the actual and extracted transistor S-parameters is computed using the formula given in [35]:

$$\text{Error} = \frac{\sum_{i=1}^{N}\sum_{j=1}^{N}\left(\frac{|S_{ijA}-S_{ijB}|}{0.5\cdot(|S_{ijA}|+|S_{ijB}|)}\right)}{N^2} \tag{2.6.1}$$

In this equation S_A and S_B are the two sets of S-parameters that are compared. In our case, N=2 since we analyze two port networks.

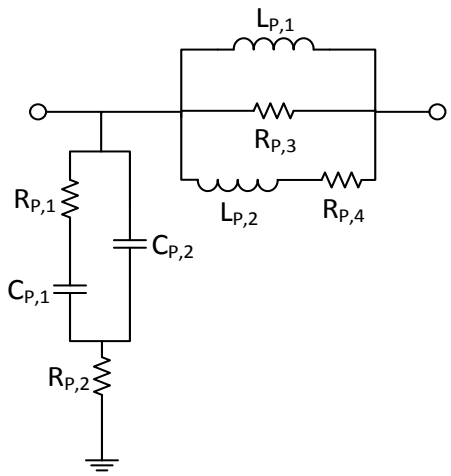
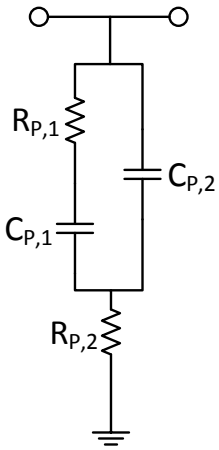
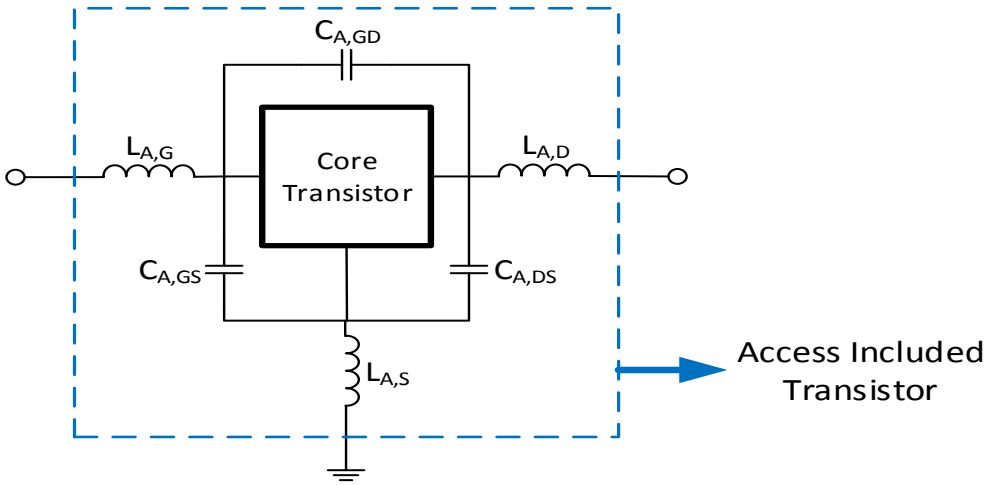
As explained before, lumped equivalent circuit model based and mixed techniques de-embed the DUT access parasitics, while cascade based techniques include those parasitics in the resultant transistor model. Therefore, for the L-NL, Alain's and open-short pads methods, which are the cascade based techniques, access included transistor S-parameters are compared with the de-embedded S-parameters; for the rest of the methods, core transistor S-parameters are compared with the de-embedded S-parameters.

Accuracy investigation of the de-embedding techniques are done for three different cases where different pad-transistor model combinations were used:

Case 1: Pad No:1 & Access included transistor
Case 2: Pad No:1 & Core Transistor
Case 3: Pad No:2 & Access included transistor

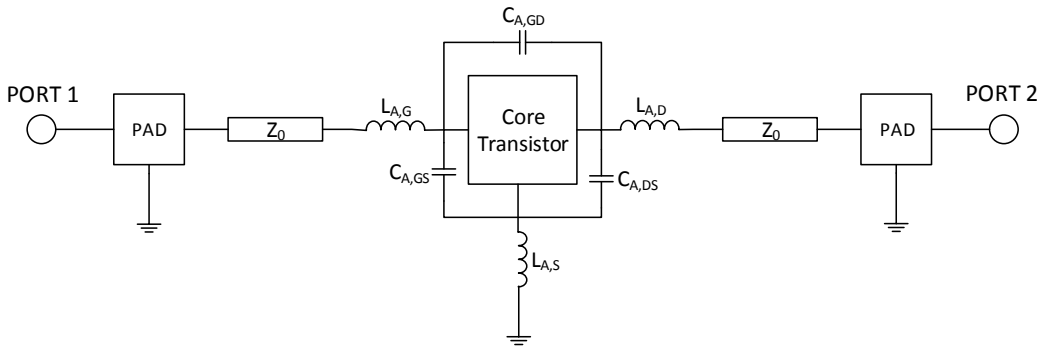
This type of an investigation is required because of two reasons. First, in microstrip environment, the effect of the access on the transistor performance is much less significant compared to its effect in CPW environment, mainly because there is no long ground connections from transistor to the side grounds as in CPW case. Besides, if the access is designed carefully, its effect can be made negligible even in the CPW environment. Second, pad structure in use can affect the accuracy of a method.

Table 2: Summary of the component models used in the simulations

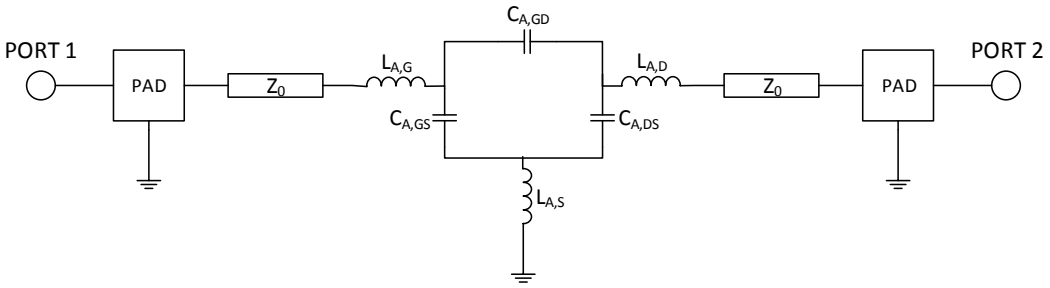
Pad Model No:1	Pad Model No:2
	
Access Model	
	
Core Transistor Model	**Transmission Line Model**
A design kit model of an 50 finger NMOS with W=45μm and L=30 nm and bias voltages $V_{DS} = 1V$ and $V_{GS} = 0.7V$	ADS TLINP model with Z=40 Ω, L=50μm, K=6, A=1000 dB/m, F=80 GHz, TanD=0.05

Case 1

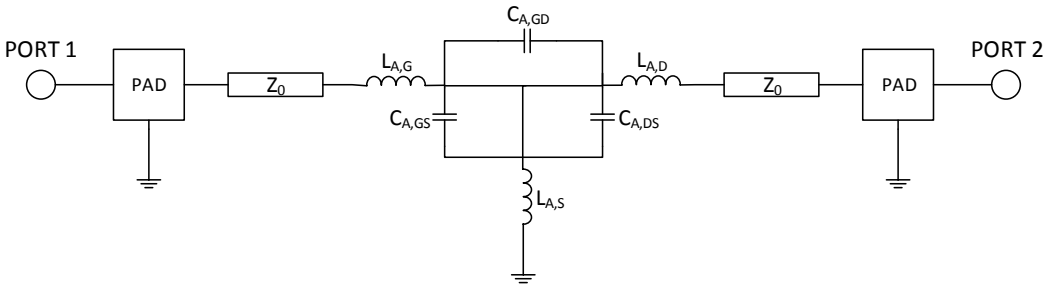
Pad No:1, access included transistor and the transmission line sections were used to build the test structure schematics shown as in Figure 2.6.1.



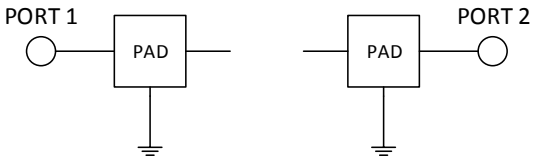
(a) DUT



(b) Open

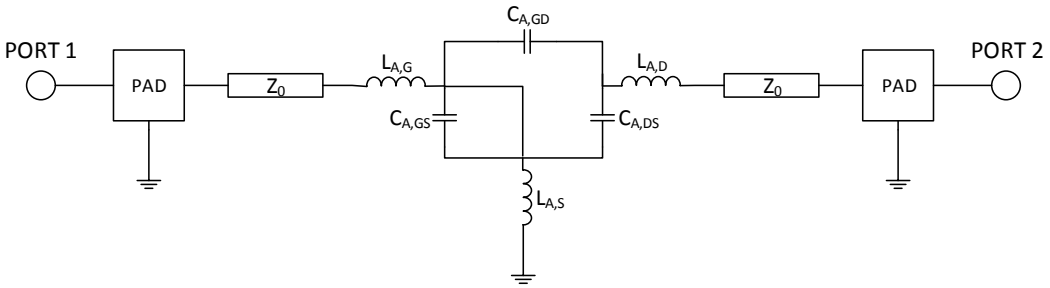


(c) Short

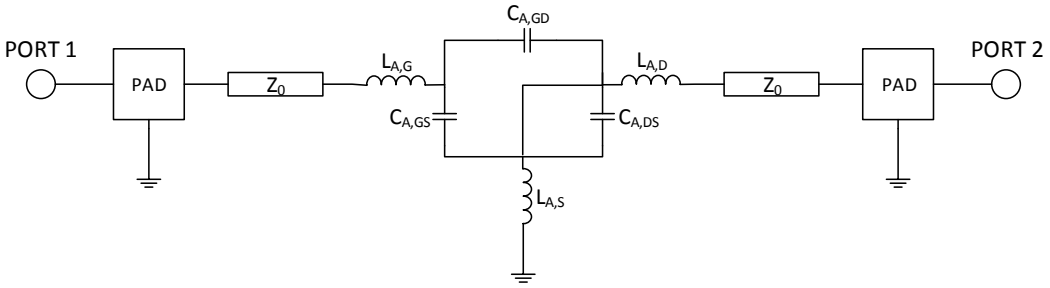


(d) Pads Only

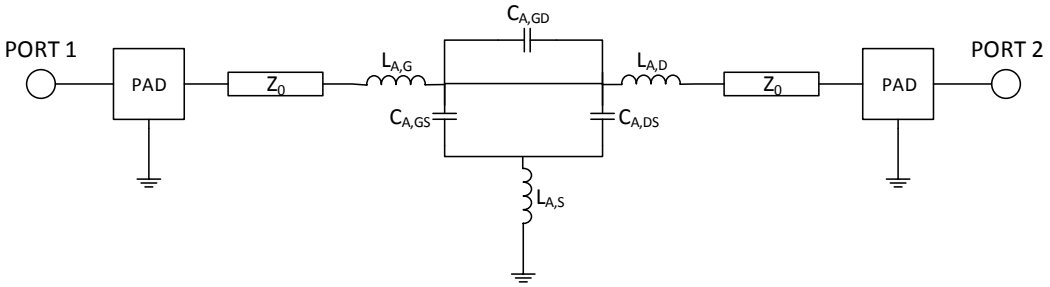
Figure 2.6.1: Schematics of the simulated test structures in the existence of transistor access



(e) Short 1



(f) Short 2



(g) Thru

Figure 2.6.1: Schematics of the simulated test structures in the existence of transistor access (cont.)

Results of the comparison between the original and de-embedded S-parameters are shown in Figure 2.6.2. As far as the access included transistor S-parameters are concerned, it is seen that the error is zero along the full frequency range for L-NL and open-short pads methods. The reason for this is that these two methods account for all parasitic effects included in the assumed pad model. However, in a real case, behavior of the pad is more complicated and the assumed model loses validity at high frequencies. In addition, it is not possible to realize ideal open-short pad structures used in the latter method, and this will introduce error too. Last but not least, a perfectly accurate measurement is not possible in real life due to the error in calibration, noise and external factors. Therefore de-embedding with zero error is not possible in reality.

It is very important to note that the results shown in Figure 2.6.2 represent the theoretical limits of the methods for given pad and access models. If different transistor, line, pad and access models were used, the results would change. The exact frequency at which a de-embedding method becomes inaccurate is a strong function of the DUT being characterized and the parasitic sources. Hence, these results can not be used to make a conclusion about the absolute accuracies of the presented de-embedding methods, but they can be used as an effective comparison tool between the methods.

Results given in Figure 2.6.2 show that L-NL and open-short pads methods are more accurate than the Alain's method in extracting the access included transistor S-parameters. Although it is small, there is a non zero error in the Alain's method mainly because it ignores the series part of the pad parasitics. But still, it stands to be a powerful tool.

As far as the core transistor S-parameters are concerned, the new method appears to be the best option with zero error. This is because it accounts for all the parasitic sources in the assumed pad and line models. Pads-short-open method is the second best option with a relatively low error up to very high frequencies. The main cause of the error in this method is that the transmission line section, which is a distributed element, is assumed to be a series impedance. Thru and thru-short methods result in high errors starting from low frequencies due to the reason that they do not account for the capacitive parasitics caused by the transistor access. It is seen that open-short and short-open methods are functional at low frequencies, however as the frequency goes higher they lose accuracy because the assumed equivalent models are not complete enough to model the whole structure. Accuracy of the three-step de-embedding is somewhere between that of the open-short and pads-short-open methods due to the reason that it partially accounts for access parasitics.

Case 2

In this case, Pad no:1, core transistor and the transmission line sections were used to build the test structure schematics. Schematics are the same as the ones in Figure 2.6.1 except $C_{A,GD}$, $C_{A,GS}$ and $C_{A,DS}$ are removed; $L_{A,G}$, $L_{A,D}$ and $C_{A,S}$ are shorted. Results of the comparison between actual and de-embedded S-parameters are shown in Figure 2.6.3.

Performances of the cascade based (L-NL, Alain's, open-short pads) methods remain the same due to the reason that their results are compared with the access included transistor model if there is an access, and with the core model if there is not, and therefore independent of presence of an access.

The new method again results in zero error because of the reason explained in the previous case.

It is seen that there is a significant improvement in the accuracies of open-short, thru, thru-short and three step de-embedding methods. Actually they all result in the same error, because assumed equivalent circuits for each method simplifies to the same circuit for this specific case.

Pads-short-open method still gives lower error compared to the other lumped equivalent circuit based and mixed techniques since it assumes a more complete

equivalent circuit. However, it is seen that the error difference between the pads-short-open and open-short methods is quite low for the whole frequency range (<%2). Hence, it can be concluded that by comparing the results from pads-short-open and open-short methods, one can deduce how effective the access is on the transistor performance. If there is a considerable difference between the results of two methods as in Case 1, access has a significant effect; if the results of two methods are in good agreement as in Case 2,then the effect of access is insignificant.

There is an enhancement in the performance of short-open method as well. However, it still fails to accurately de-embed the transistor at high frequencies,and therefore it is suitable only for low frequencies.

Case 3

Pad No:2, access included transistor and the transmission line sections were used to build the test structure schematics shown as in Figure 2.6.1. Results of the comparison between actual and de-embedded S-parameters are shown in Figure 2.6.4.

This time Alain's method also gives zero error for the whole frequency range together with the L-NL and open-short pads methods. This is because the assumed pad model (Pad No:2) does not have a series component which was the source of the error in the previous cases for the Alain's method. In a real case, if the L-NL method is preferred for de-embedding purpose, one can employ the Alain's method as well using the same test structures and make a conclusion about the impact of the series parasitic component of the pad. If the results from two methods appear to be in good agreement, it means that the pad can be modeled as a single shunt admittance for the frequency range of interest.

Accuracies of the rest of the methods are similar to the results in Case 1, since the effect of the series component of the pad on those methods is negligible.

Final Comments

The simulation results presented in this section show that the new de-embedding method is superior over most of the well known, older techniques in terms of accuracy. One of, if not the most important feature of this technique is that it characterizes not only the DUT, but also the DUT access which can be quite useful in circuit design. In the next chapter, the new de-embedding technique will be used to characterize manufactured test structures and measurement results will be provided to verify this technique.

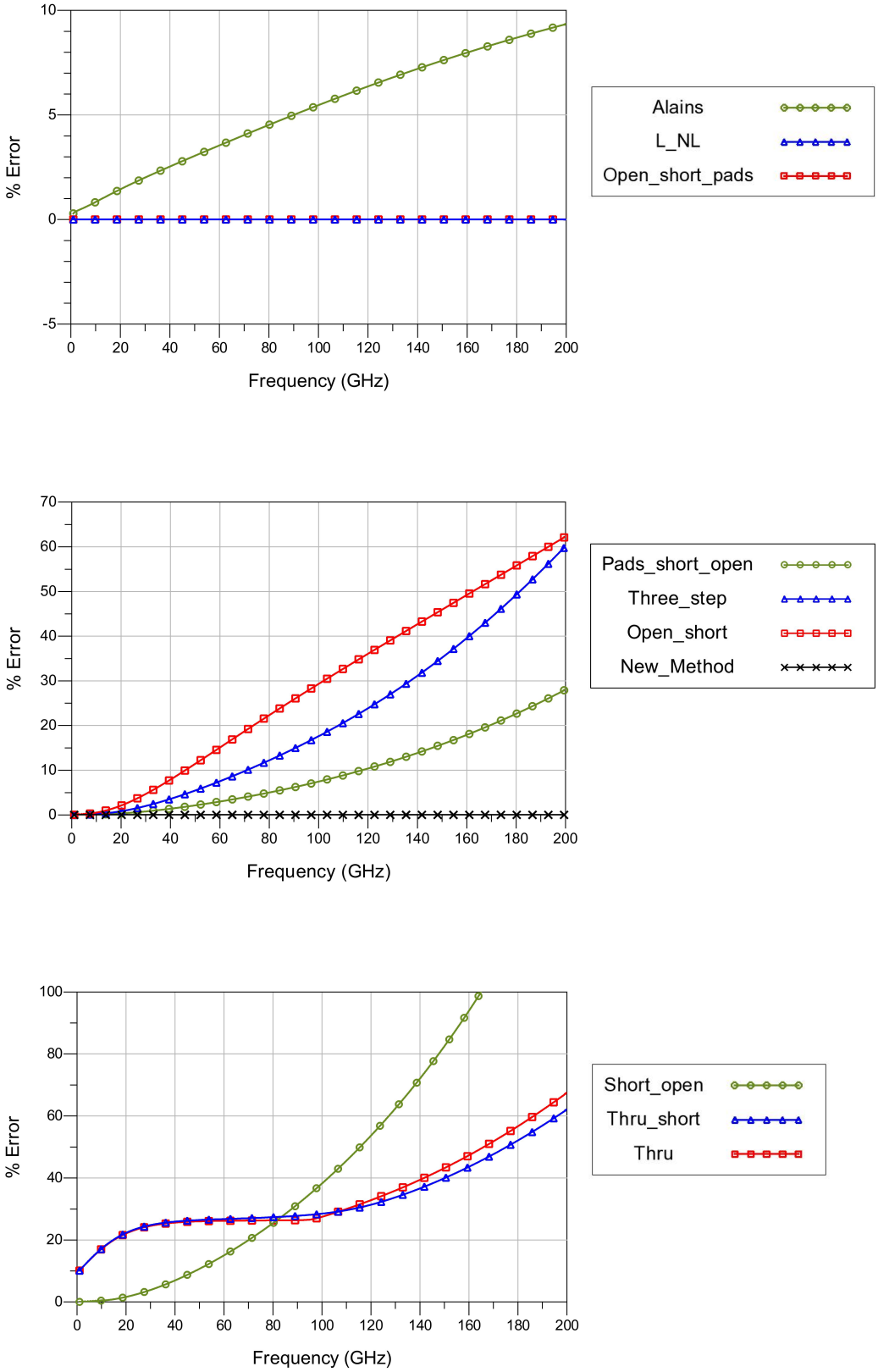


Figure 2.6.2: Percentage errors resulting from different de-embedding techniques in Case 1

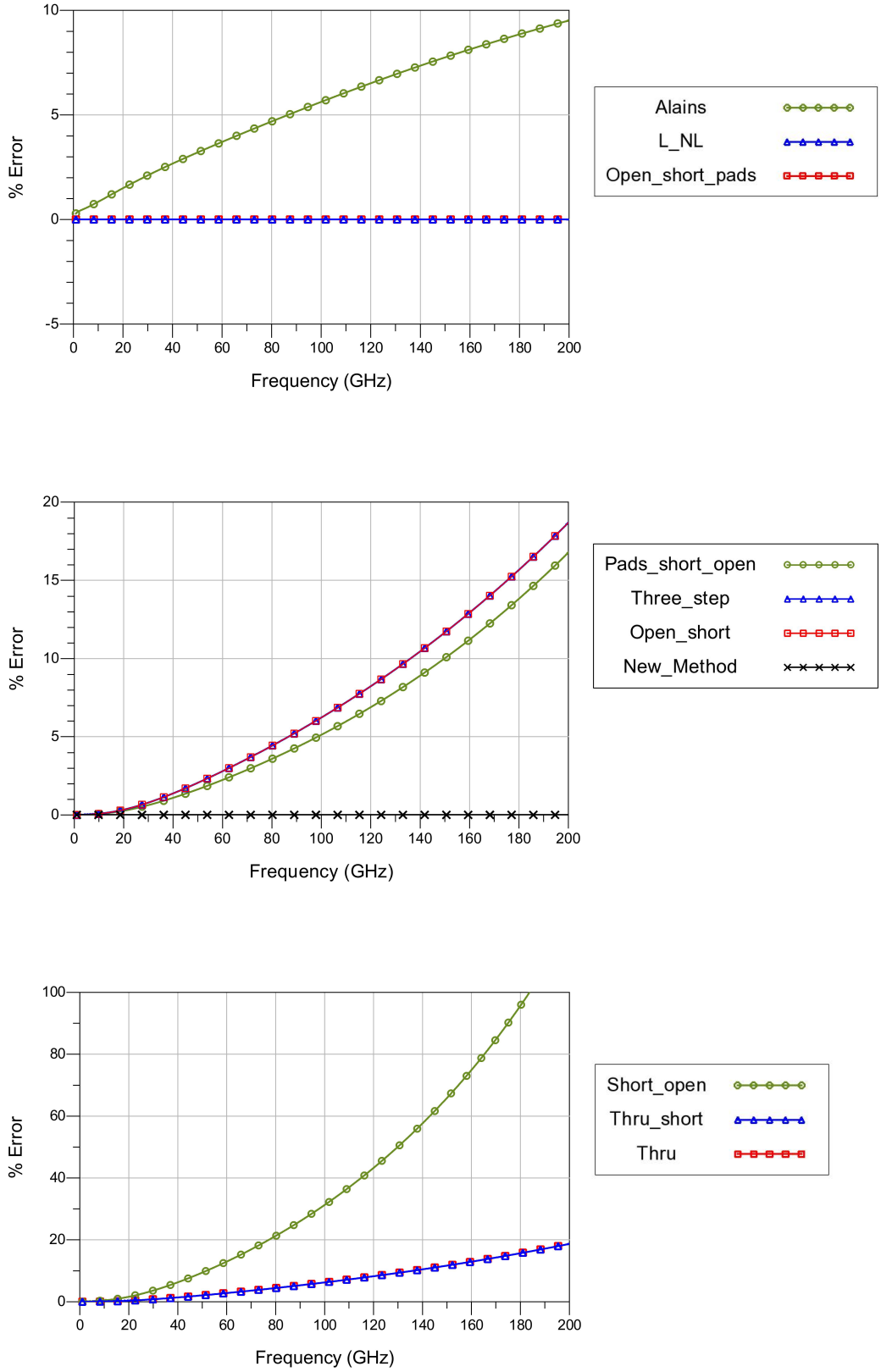


Figure 2.6.3: Percentage errors resulting from different de-embedding techniques in Case 2

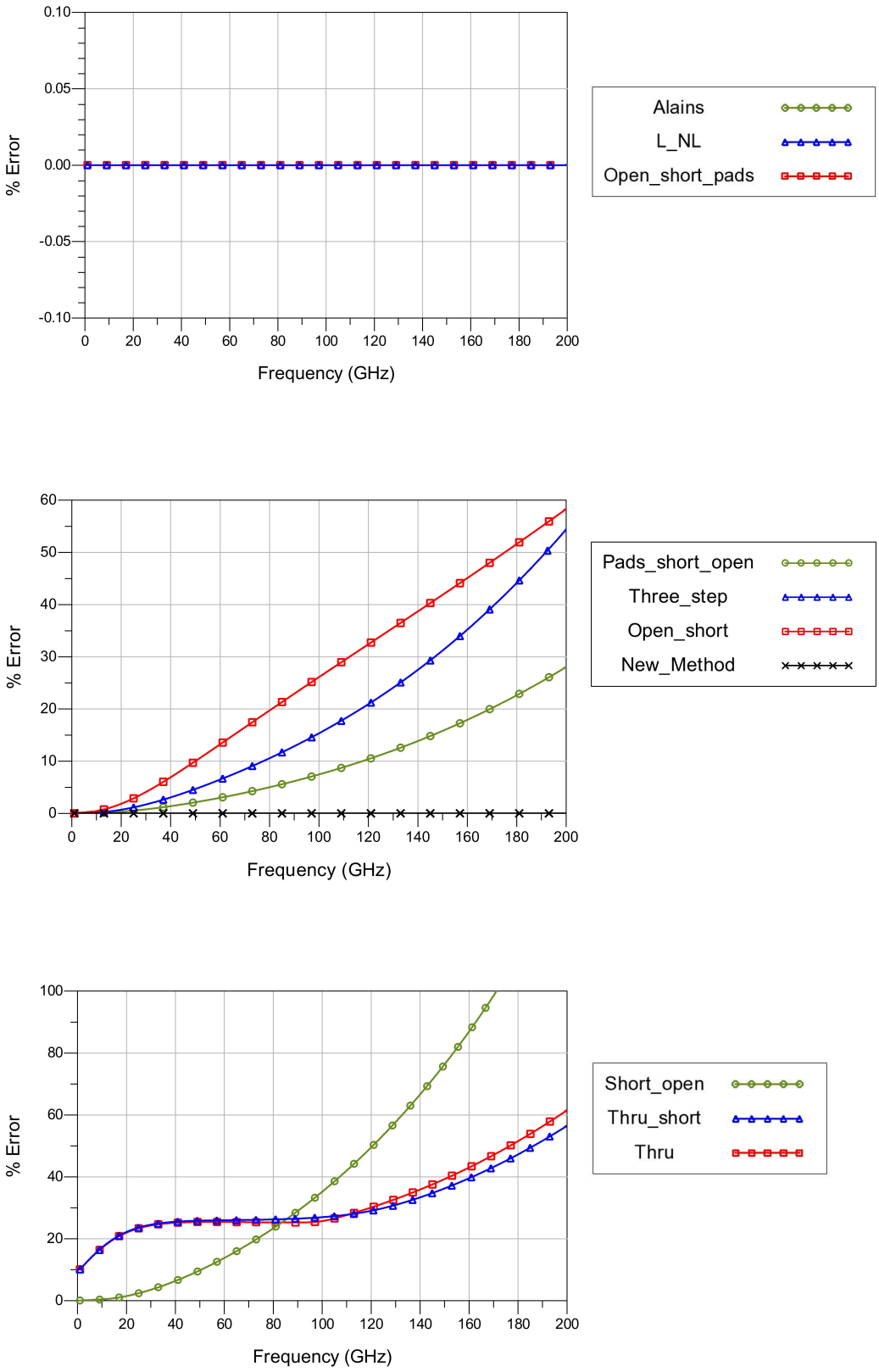


Figure 2.6.4: Percentage errors resulting from different de-embedding techniques in Case 3

3 Measurement Results and Characterization of the Test Structures

3.1 Introduction

Measured results of various test structures fabricated in 28-nm FDSOI CMOS technology are analyzed to characterize passive and active devices using the de-embedding techniques explained in the previous section. The chip used in this study had been manufactured before the study started, so it was not possible to choose the test structures to be manufactured. Available test structures on the chip were:

- Open and short pads
- A slow-wave co-planar transmission line section of length 216μm
- Two DUT structures for 2x12 and 2x25 sized transistors (For an AxB sized transistor, A is the gate split and B is the number of fingers per gate split. Width of a single finger is 0.9 μm.).
- Open and short test structures for the DUTs.

3.2 Pad

Probe pads on the chip are in GSG configuration with 100μm pitch and they do not have a metal shield underneath. Therefore, they require careful characterization as they are likely to have substantial substrate loss [36]. Open and short pad measurements are used to extract the two port parameters of the probe pad as explained in section 2.3.3. To be able to use the pad model at frequencies higher than the maximum frequency of measurement, a circuit with lumped elements can be adopted as a pad model. Since the substrate losses are involved, building an equivalent circuit becomes more difficult. Circuit shown in Figure 3.2.1 is used to model the GSG pad. The resistor, capacitor and inductor values are optimized to obtain a simultaneous Z parameters fit between the model and the measurement for open and short cases.

Figures 2.5.2 and 3.2.3 show the measured vs. simulated Z parameters fit for open and short cases, respectively. It is seen that there is a very good agreement between the measured and simulated results. This indicates that the proposed lumped model can successfully model the probe pad up to 110 GHz.

In order to prevent the substrate losses, which degrades the RF performance of the probe pad significantly, as well as to simplify the modeling, a metal shield should be implemented under the probe pads. The design of a shielded RF probe pad will be shown in section 4.5.

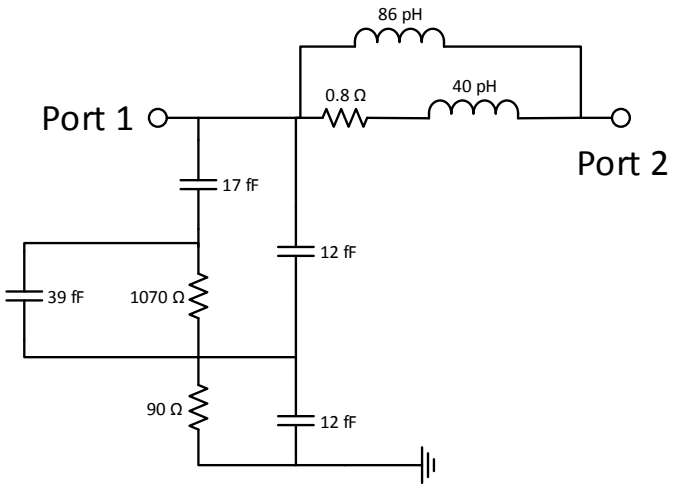
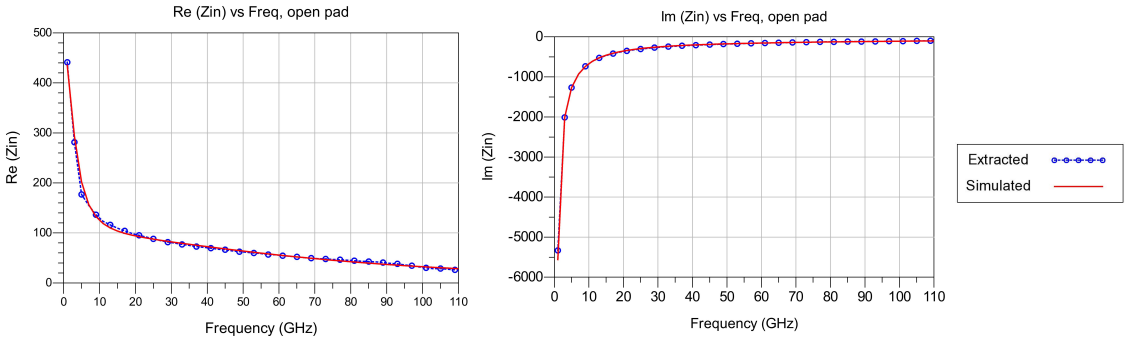
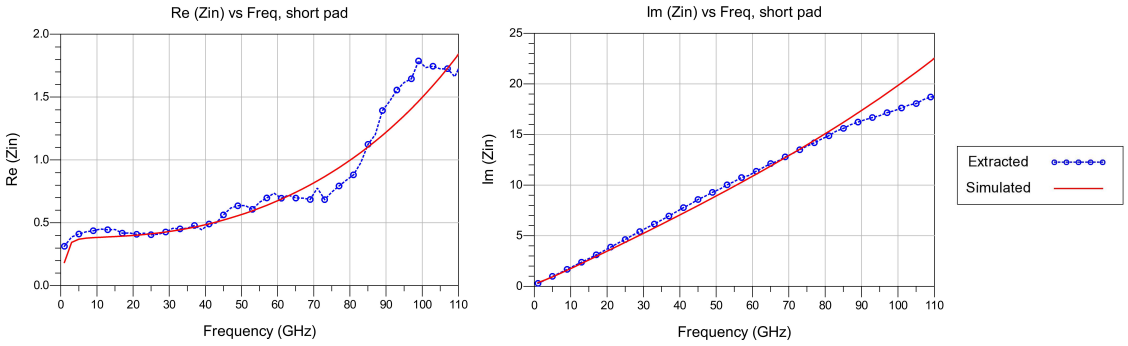


Figure 3.2.1: Lumped model of the RF pad



(a) (b)

Figure 3.2.2: Measurement vs. model results for the GSG RF pad with port 2 open. Real(a) and imaginary(b) parts of Z_{in} (derived from single port S-parameters).



(a) (b)

Figure 3.2.3: Measurement vs. model results for the GSG RF pad with port 2 grounded. Real(a) and imaginary(b) parts of Z_{in} (derived from single port S-parameters).

3.3 Transmission Line

Slow-wave co-planar wave guides (S-CPW)[1] were used as interconnects on the chip. Using the lumped pad model developed in the previous section, pad parasitics were removed from the transmission line measurement with the help of cascade based methods explained in section 2.3. First, equations from 2.3.8 to 2.3.15 were used to obtain ADS TLINP transmission line model parameters from the extracted two-port parameters of the line. Calculated values of the model parameters are Z=40.2 Ω, K=6.4, A=800 dB/m, TanD=0.07, F=90 GHz. Then, the TLINP model parameters were optimized such that the measured S-parameter data fits the simulated one. Optimized values of the model parameters appeared to be very close to the calculated ones as expected, and they are Z=40.4 Ω, K=6.3, A=900 dB/m, TanD=0.06, F=92.4 GHz. Figure 3.3.1 shows the measured and simulated S-parameter fit for the line section. Good agreement is obtained between the model and the measurement over a wide frequency range.

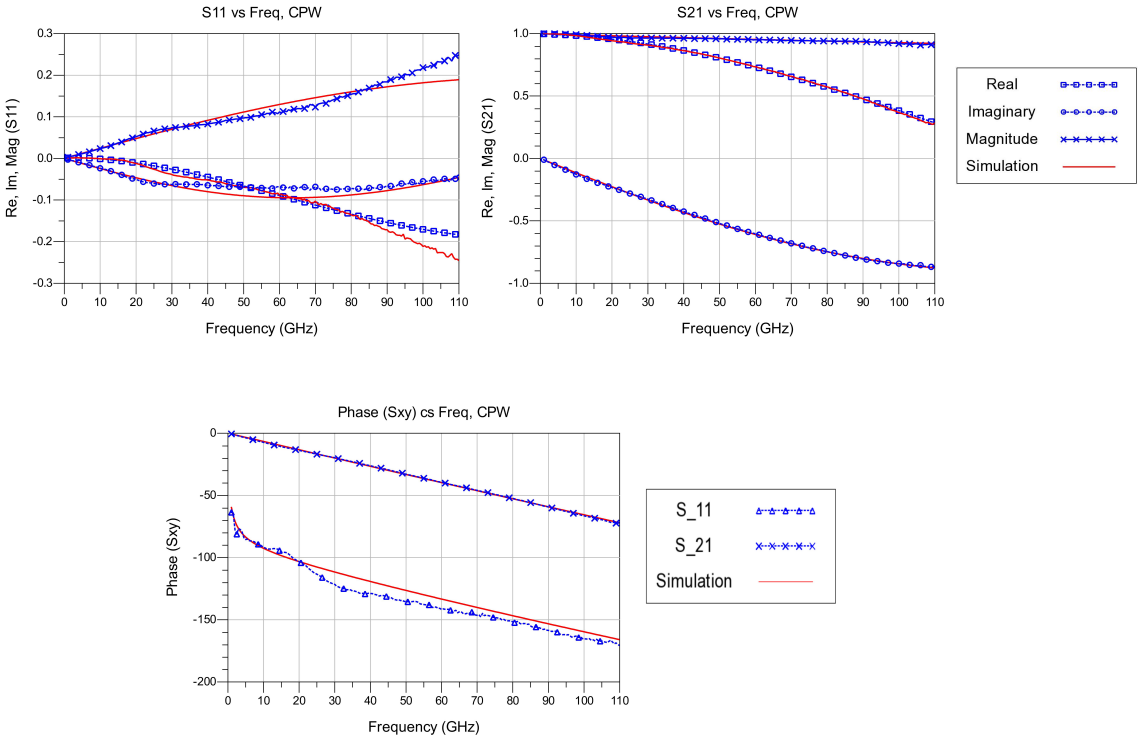


Figure 3.3.1: Measured vs. simulated S-parameters fit for the slow-wave co-planar waveguide

[1]See chapter 4.2 for more details about S-CPW.

3.4 Core Transistor

With the existing test structures on the chip, it is possible to carry out open-short, pads-short-open and the proposed new de-embedding technique. In this section, all three methods are carried out and extracted models are compared to the simulated post layout design kit models.

First, open-short method is carried out and extracted results are compared to the design kit model in Figures 3.4.1 and 3.4.2. It is seen that the extracted parameters and the simulated design kit model do not agree above 60 GHz. If these results are not interpreted carefully, one might think that the design kit model is not valid above 60 GHz, which is a wrong conclusion. In fact, the inconsistency between the two results is mainly because open-short de-embedding fails to account for the transistor access parasitics at high frequencies.

As discussed in section 2.6, pads-short-open method should de-embed the access parasitics, so we continue our analysis with pads-short-open de-embedding. Due to the absence of a pads-only test structure on the chip (Fig. 2.2.4), an alternative strategy was used to carry out pads-short-open de-embedding. Considering that the coupling between two pads (between port 1 and port 2) is negligible, Y_{P3} parameter in the lumped equivalent circuit of the pads-only test structure (Fig. 2.2.5d) is assumed to be zero. In this case, the admittance matrix of a pads-only test structure can be written as,

$$[Y_{pad}] = \begin{bmatrix} Y_p & 0 \\ 0 & Y_p \end{bmatrix} \tag{3.4.1}$$

where Y_p is the measured admittance of the open pad structure. After forming the admittance matrix of a virtual pads-only test structure, pads-short-open de-embedding method is employed and core transistor S-parameters are extracted. Figures 3.4.3 and 3.4.4 show the comparison between extracted model and post layout design kit model of the 2x12 and 2x25 sized transistors respectively. The good agreement between the results indicate that the post layout design kit models for the transistors in strong inversion are reliable at least up to 110 GHz for 28-nm technology node.

Finally, core transistor model is extracted using the new de-embedding method presented in section 2.5 in order to verify its validity. Figures 3.4.5 and 3.4.6 show the extracted vs. simulated design kit model S-parameter fit for 2x12 and 2x25 sized transistors respectively. It is seen that there is a good agreement between the extracted and simulated results meaning that the proposed de-embedding technique is an effective way for characterization of devices up to 110 GHz.

Pads-short-open and proposed technique successfully de-embeds the transistor while the open-short method fails to do so above 60 GHz. This shows that the transistor access has a significant impact on the transistor performance at higher frequencies. Therefore, access characterization is needed and will be presented in the next section.

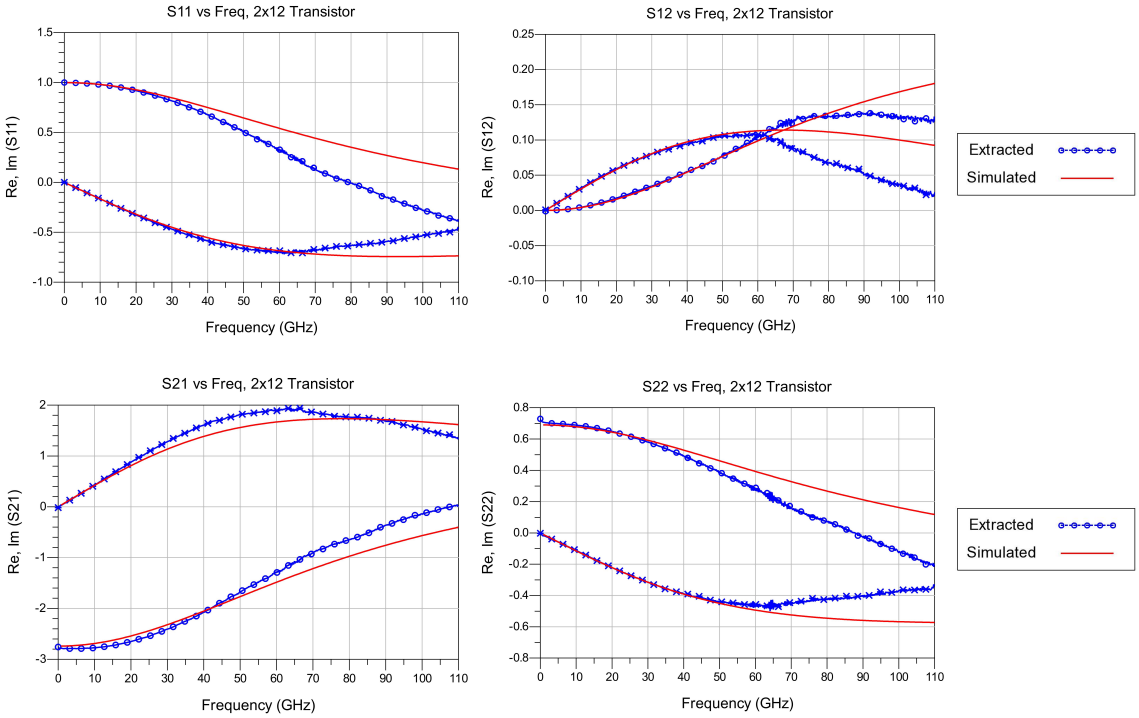


Figure 3.4.1: Extracted (using open-short method) vs. design kit model S-parameters for the 2x12 sized transistor

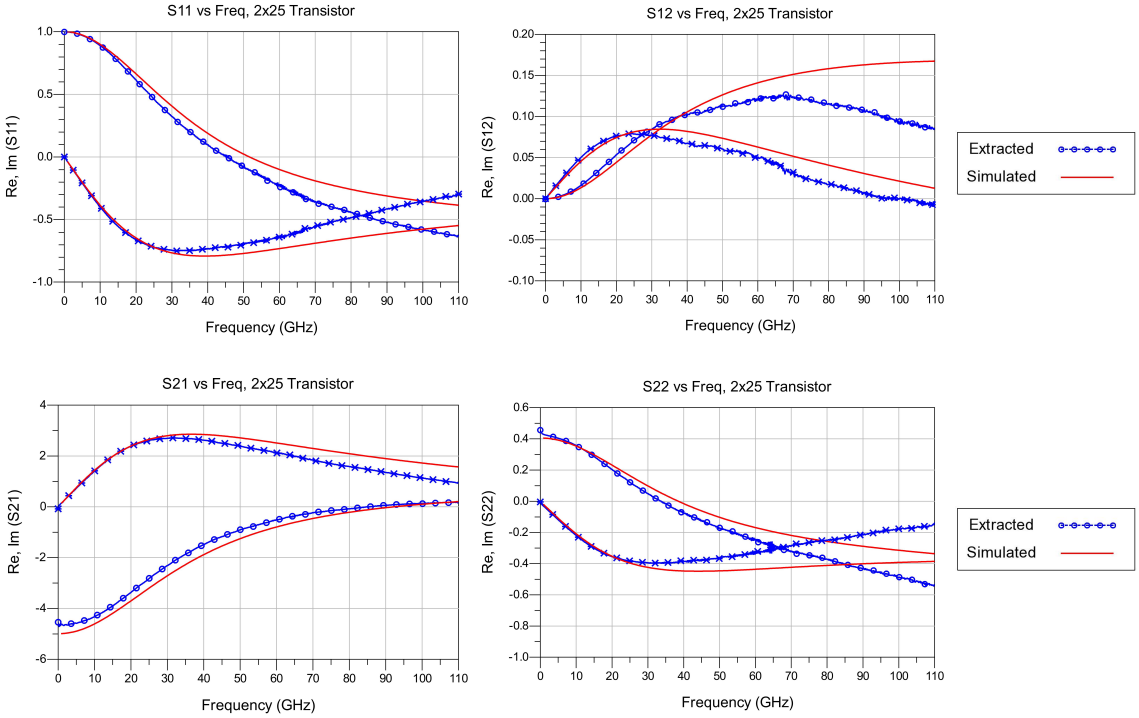


Figure 3.4.2: Extracted (using open-short method) vs. design kit model S-parameters for the 2x25 sized transistor

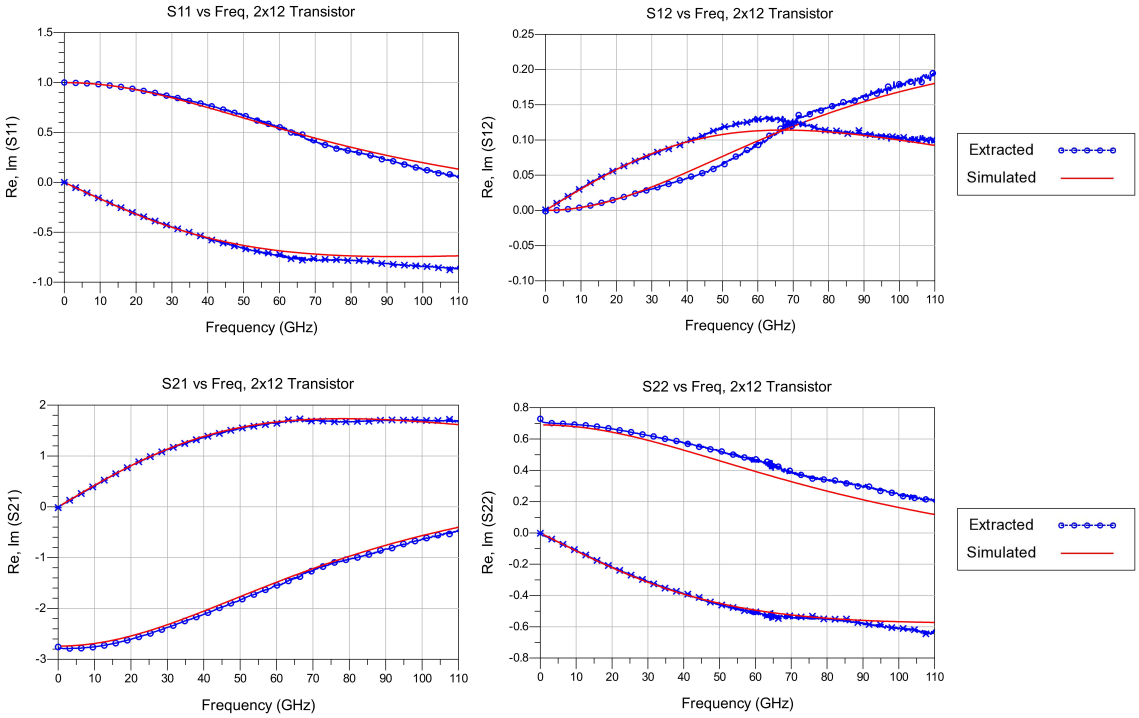


Figure 3.4.3: Extracted (using pads-short-open method) vs. design kit model S-parameters for the 2x12 sized transistor

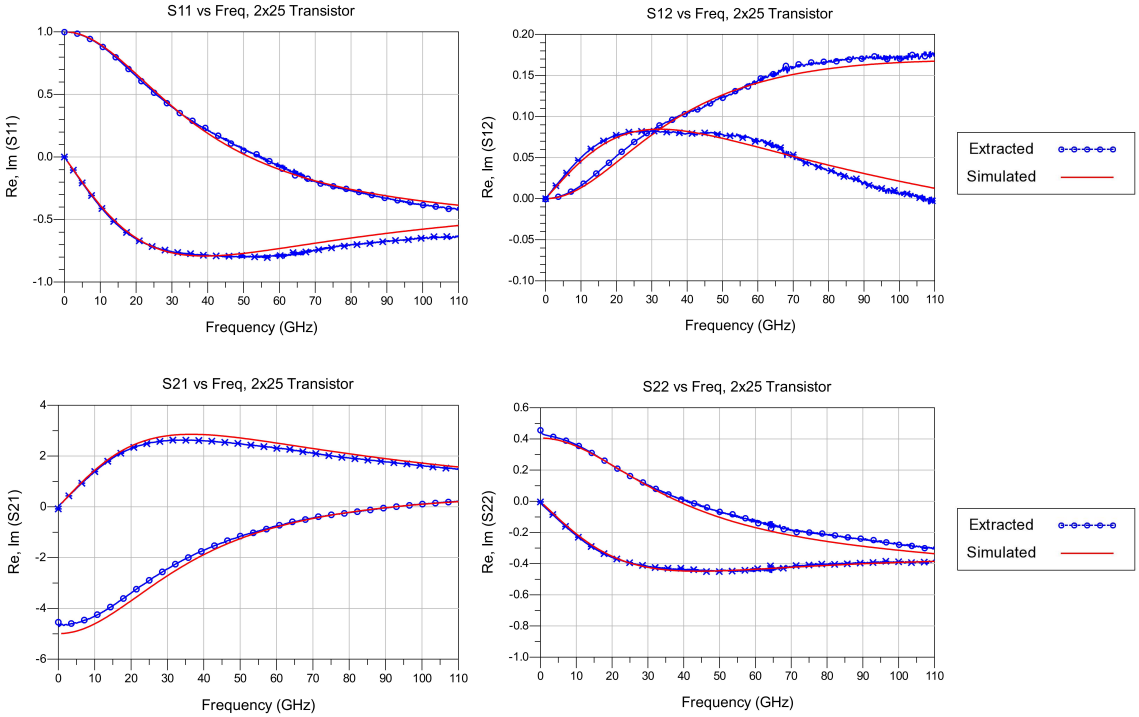


Figure 3.4.4: Extracted (using pads-short-open method) vs. design kit model S-parameters for the 2x25 sized transistor

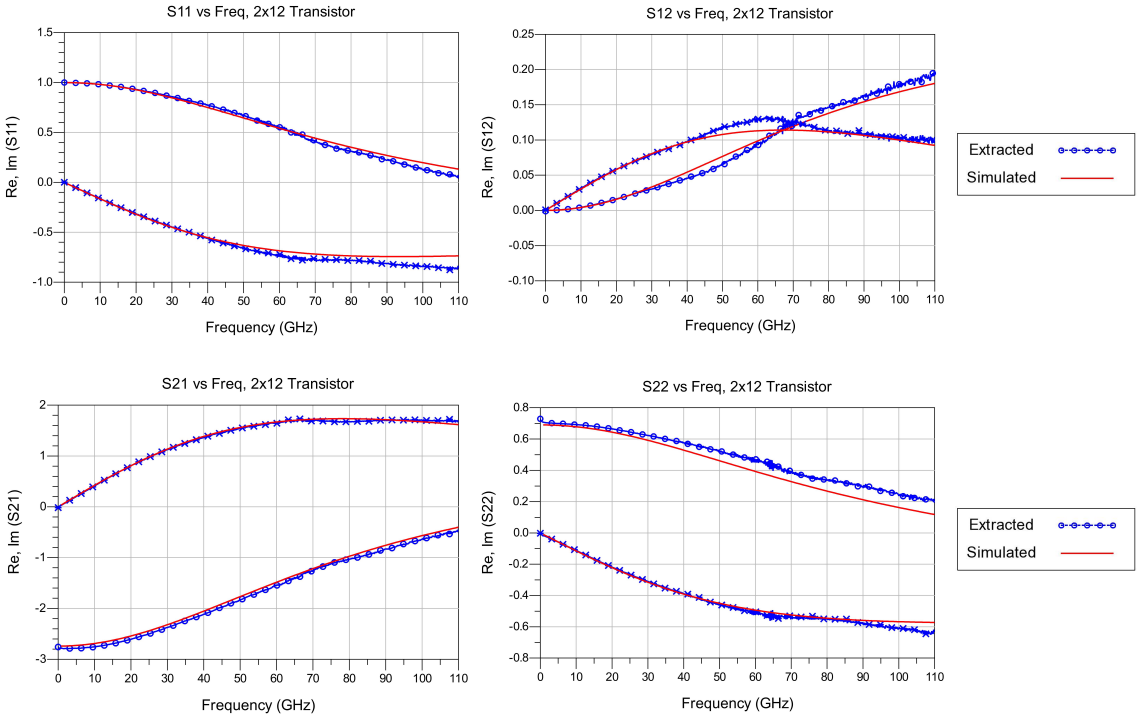


Figure 3.4.5: Extracted (using the new method) vs. design kit model S-parameters for the 2x12 sized transistor

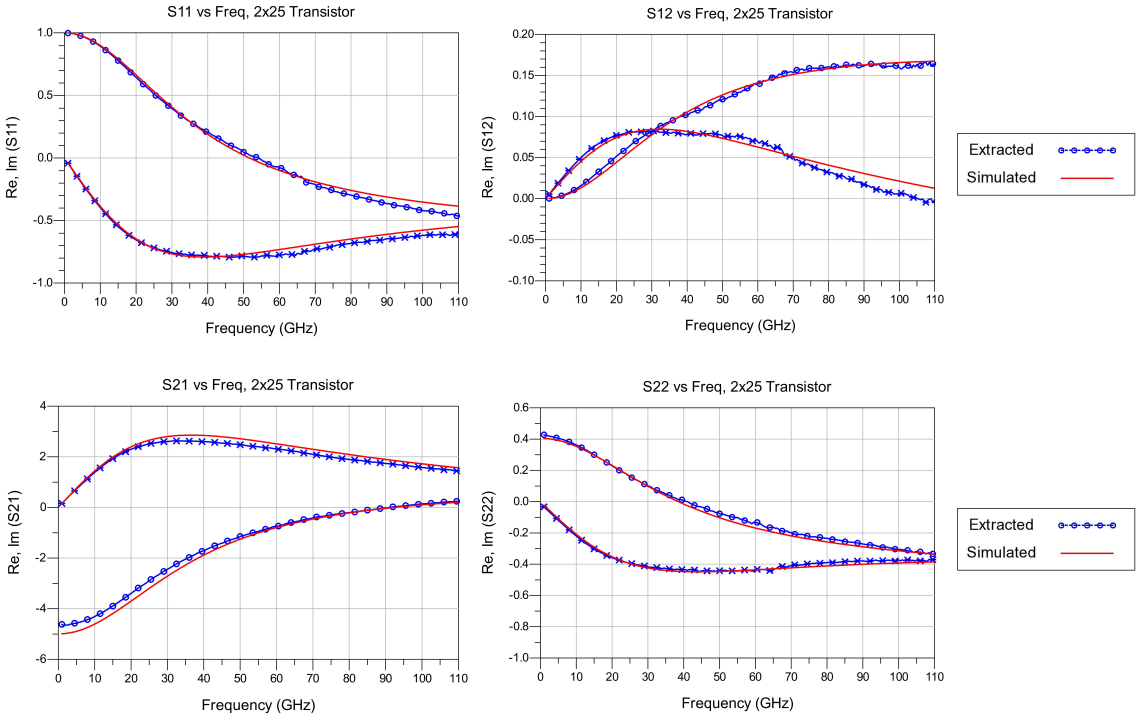


Figure 3.4.6: Extracted (using the new method) vs. design kit model S-parameters for the 2x25 sized transistor

3.5 Transistor Access

In this section, access characterization is explained and its validity is investigated. As stated in the previous section, results from open-short and pads-short-open de-embedding methods do not agree with each other above 60 GHz indicating that the access parasitics has a significant impact on the transistor performance. Characterization of the access parasitics is important, as they alter f_t and f_{max} values of the transistor, as well as the matching conditions by affecting the input and output impedances of the transistor.

Using the pad and line models developed in sections 3.2 and 3.3, the new method proposed in section 2.5 is carried out and the access model consisting of Z_1, Z_2, Z_3, Y_1, Y_2, Y_3 is extracted (Fig. 2.2.3a). To be able to use the access model at frequencies higher than the maximum frequency of measurement, a circuit with lumped elements can be adopted as the access model. In Figure 3.5.1, adopted lumped circuits and extracted vs. simulated Z-Y parameters fits are shown for Y_1, Y_2 and Z_3. Extracted values of Z_1, Z_2 and Y_3 were negligible, so they are not included in the lumped model. The analytical calculation of the lumped component values can be found in [12], where these lumped circuits were originally used to model the coupling between probe pads instead of the DUT access.

To verify the proposed access characterization method, both for 2x12 and 2x25 transistors, core transistor models from the design kit are combined with the developed access model, simulated and compared to the access included transistor model extracted via open-short pads method (Fig 3.5.2 and 3.5.3). It is seen that a very good agreement between the two results is obtained, indicating that the proposed access characterization method is an effective tool at least up to 110 GHz.

As it has been shown in this and previous sections, the DUT access used in the manufactured test structures has a noteworthy effect on the measured transistor two-port parameters, mainly because its relatively large size compared to the core transistor. Because of the parasitic effect of the DUT access, the high frequency performance of the transistor worsen, and the modeling of the transistor becomes more complex. Therefore, in the new transistor design, which will be presented in section 4.6, use of a physically large transistor access is avoided.

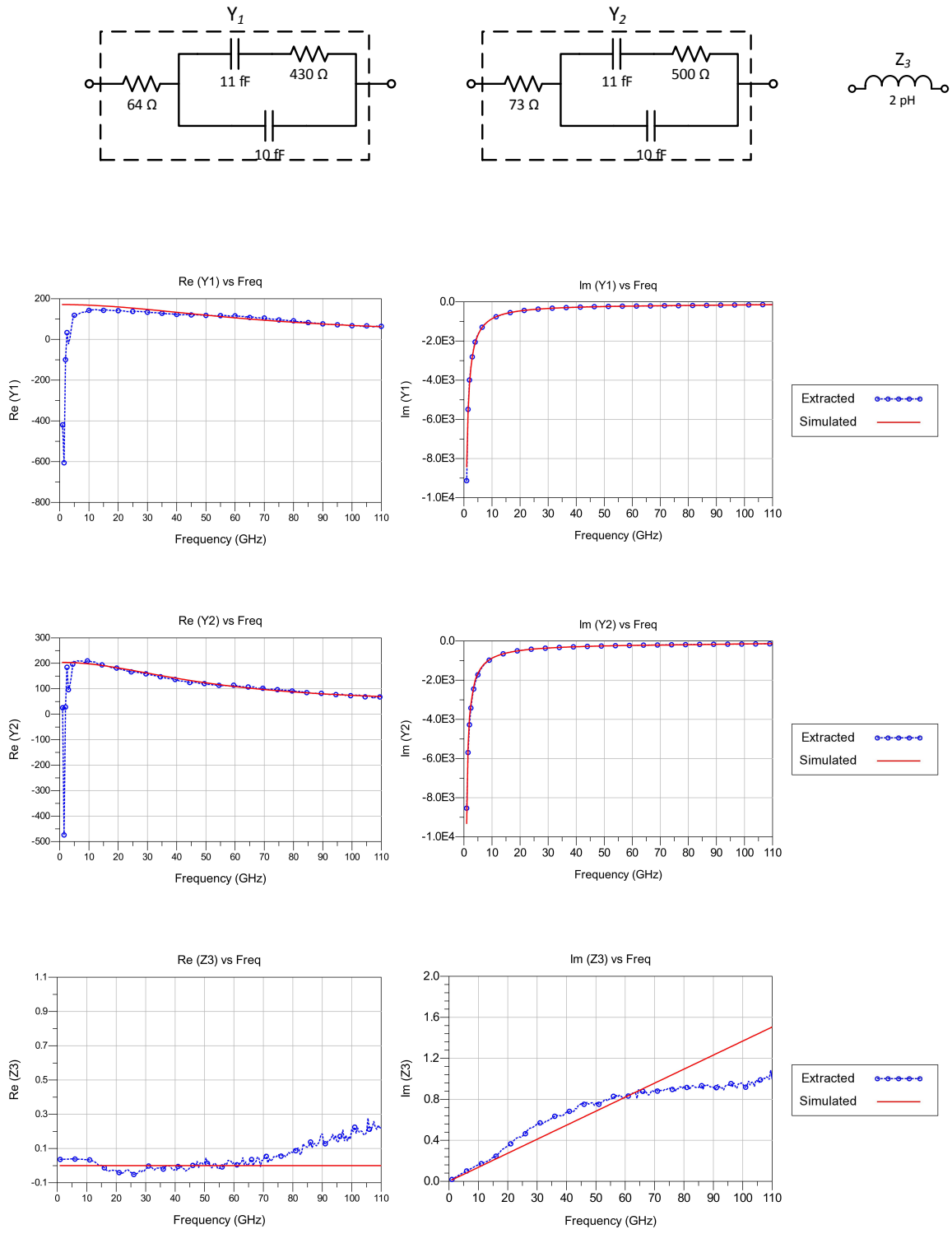


Figure 3.5.1: Equivalent models of the access components Y_1, Y_2 and Z_3, simulation vs. extracted results

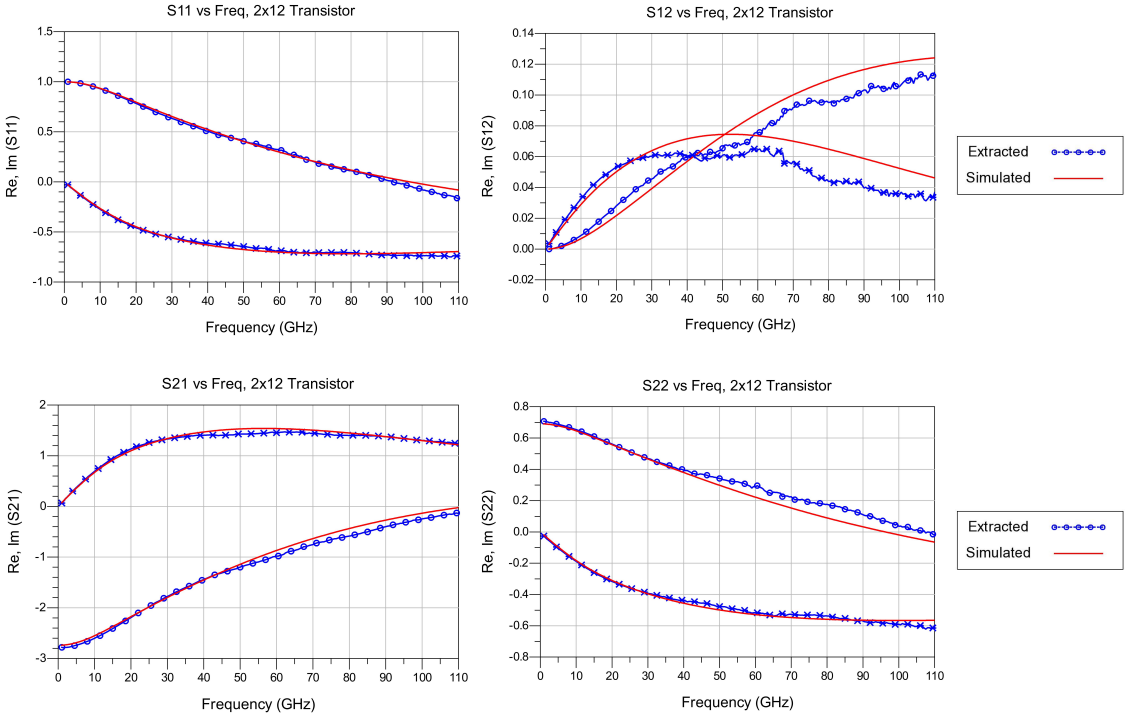


Figure 3.5.2: Extracted access included transistor model (using open-short pads method) vs. simulated core transistor+access model obtained using the new de-embedding method for the 2x12 sized transistor

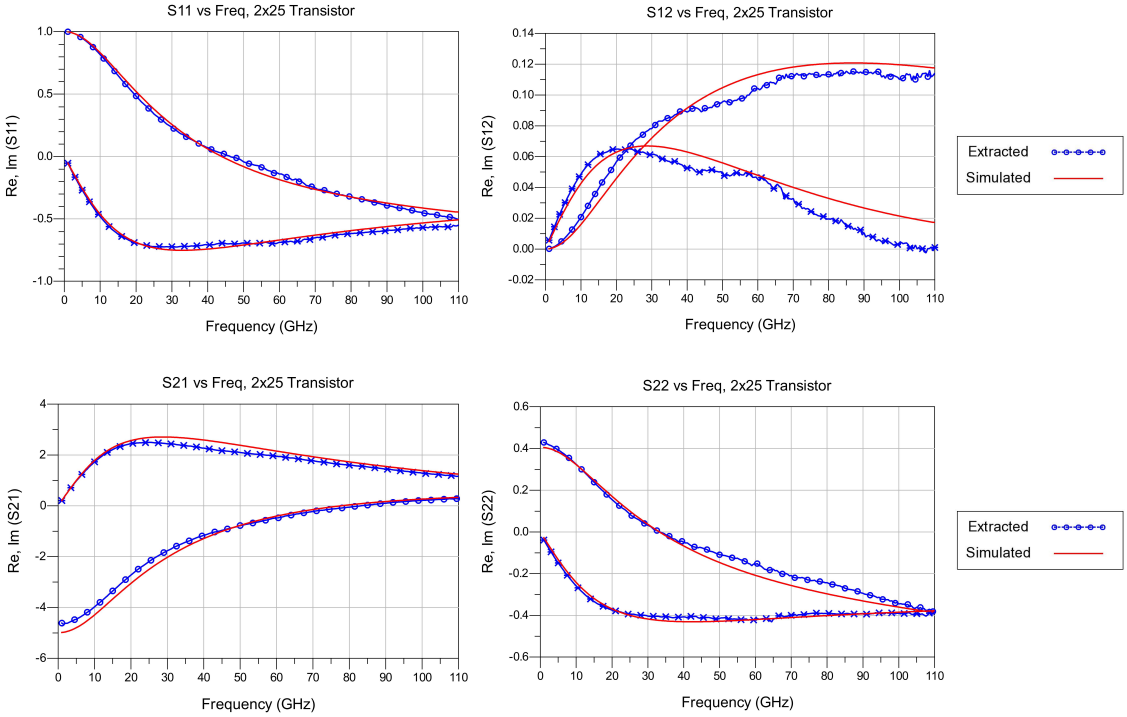


Figure 3.5.3: Extracted access included transistor model (using open-short pads method) vs. simulated core transistor+access model obtained using the new de-embedding method for the 2x25 sized transistor

4 Millimeter-Wave Passive and Active Component Design

At mm-wave frequencies it is of great importance to choose the active and passive devices such that the design is efficient and the performance is good. This chapter discusses the design, optimization and modeling of mm-wave passive and active devices in detail. First a brief overview of the back-end of line (BEOL) of the 28-nm FDSOI technology, in which the devices are designed, is given. Then a comparison is made between component design in CPW environment and component design in microstrip environment, advantages and disadvantages for both cases are pointed out. The design and modeling of the transmission lines, capacitors, RF pads and transistors, which will be utilized in the design of a W-band low-noise amplifier presented in section 5, are covered.

4.1 28-nm FDSOI CMOS Back-end of Line

The cross section of the 28-nm FDSOI CMOS technology BEOL is shown in Figure 4.1.1. The exact geometry is not given due to confidentiality reasons. There are 11 metal layers above the device layer built using copper, except the thick aluminum top metal ALUCAP. M7 and M8 layers are twice, M9 and M10 layers are eight times as thick as the layers from M1 to M6. Also the dielectric thickness between to consecutive metal layers is increased at higher levels (D4>D3>D2>D1). Due to the reason that ALUCAP layer is not planarized, it is not utilized in the passive structures designed in this work, except for the probe pads. The total dielectric thickness between M10 and device layer is around 4μm.

4.2 CPW vs Microstrip Design

There are several advantages of using transmission lines for the matching networks in MMIC design. For an effective dielectric constant of 4, quarter wavelength of the on-chip signal is between 340 and 500μm in W-band. Thanks to this, it is possible to realize electrically long transmission lines on the chip, and therefore sections of transmission lines can be used as matching elements. Moreover, reactance of a transmission line is more predictable and less influenced by surroundings compared to that of a lumped spiral inductor. Next, transmission lines can be designed to obtain a particular characteristic impedance to improve the performance. Last but not least, scalability of the transmission lines makes them great tools for mm-wave design. If lumped components are utilized, each component with a different value has to be modeled individually which increases the time spent on modeling considerably.

The inductive and capacitive quality factors (Q_L and Q_C) are the two figures of merit defining the performance of a transmission line. Q_L and Q_C can be expressed in terms of distributed transmission line model parameters and frequency in radians

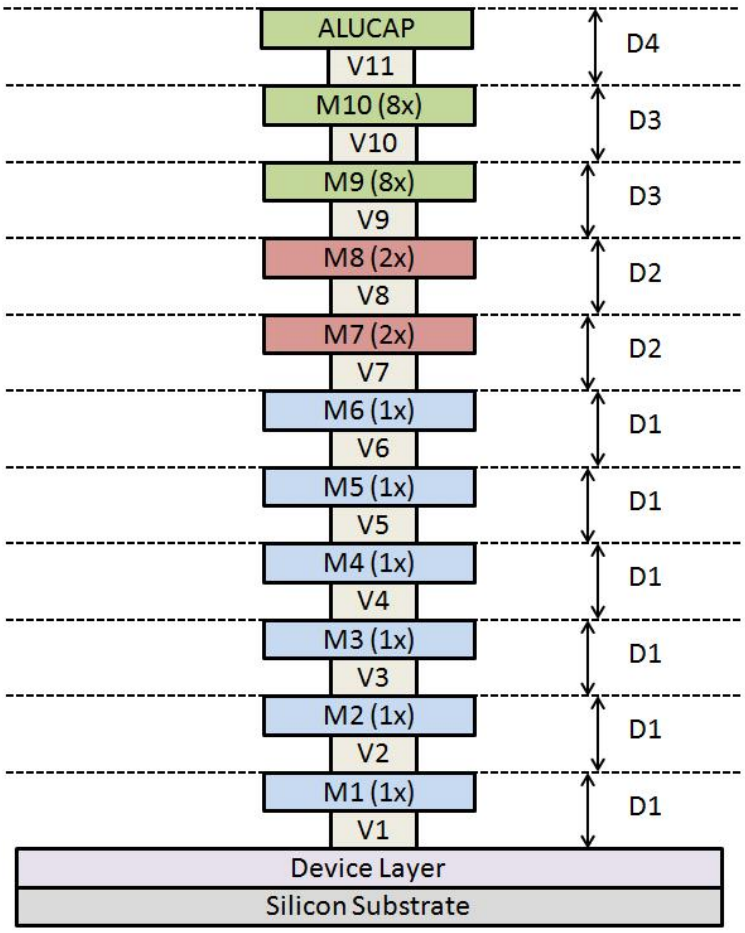


Figure 4.1.1: 28-nm FDSOI CMOS process metal stack

as follows,

$$Q_L = \frac{wL_d}{R_d} \tag{4.2.1}$$

$$Q_C = \frac{wC_d}{G_d} \tag{4.2.2}$$

where R_d, L_d, G_d and C_d are the distributed transmission line model parameters shown in Figure 4.2.1. In [37] it is stated that Q_L is more important than Q_C when transmission lines are used to match the intrinsic capacitances of the transistors. For microstrip lines it is not possible to increase L_d arbitrarily by increasing the distance between the signal line and the ground plane, because the distance between the topmost and the bottommost metal layers is fixed for a certain technology. Moreover, using bottom metal layers as the ground plane has two disadvantages. First, bottom metal layers are thinner, and therefore the microstrip lines suffer from high conductive losses, i.e. R_d is high. Second, maximum width of the bottom metal layers is typically low in CMOS technologies that a gridded ground plane has to be used which will also increase R_d. On the other hand, in CPW environment, it is possible to adjust

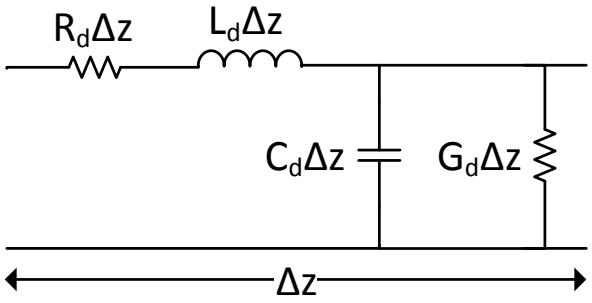


Figure 4.2.1: Lumped-element equivalent circuit for an incremental length of transmission line

L_d by changing the distance between the signal and ground lines. Thanks to this, a higher inductive quality factor can be obtained with CPWs than with microstrips. However, as the distance between the signal and ground lines increases, substantial loss arises due to low resistivity silicon substrate and G_d becomes higher. To prevent electromagnetic fields from penetrating into the lossy substrate, a metal shield can be implemented at the lower metal layers [36],[38] as shown in Figure 4.2.2.

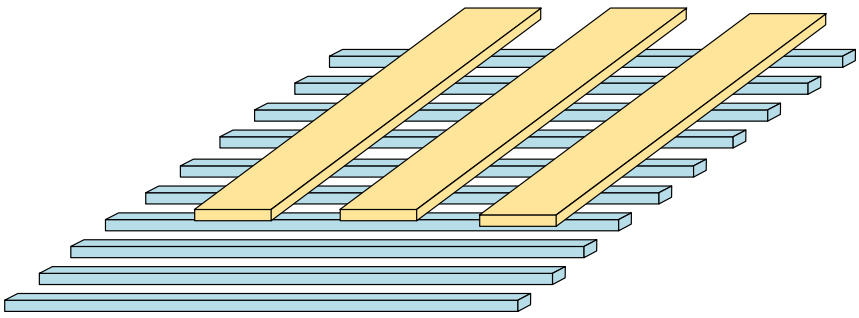


Figure 4.2.2: Shielded (slow-wave) co-planar wave guide

Resulting structure is called as slow-wave co-planar wave guide (S-CPW). When the substrate is shielded, capacitive quality factor increases inherently as C_d increases and G_d decreases, while the inductive quality factor remains the same as it is in regular CPW, since the signal and ground return current paths do not change. Inductive quality factor can be increased further by increasing the signal to ground spacing, because the substrate loss is prevented by the shield.

As discussed above, S-CPW has superior characteristics over microstrip with higher inductive and capacitive quality factors. In addition, S-CPW structure presents slow-wave effect, and therefore the effective dielectric constant is increased and the wavelength of the propagating signal is decreased. This enables the designer to use shorter line sections for matching and save silicon area. However modeling of passive structures in S-CPW environment using electromagnetic simulations is complex and time consuming. In [39], a simpler procedure, which divides the electromagnetic

problem into two parts by simulating for R_d-L_d and for G_d-C_d separately, was proposed to characterize S-CPWs. However, to be able to get accurate results from this technique, designer must ensure that there is no dummy metal generated between the signal and ground lines. In this case it might be difficult to obtain a strong slow-wave effect since it is not possible to increase the gap between signal and ground lines arbitrarily and fulfill the minimum metal density requirements at the same time. Furthermore, again as stated in [39], a floating shield might not provide adequate substrate isolation and result in significant substrate loss especially at high frequencies.

In CPW environment, modeling of shielded passive components, such as pads, capacitors and inductors, is even more challenging and cumbersome than modeling of shielded co-planar wave guides, as there no simplified simulation method for these structures. To analyze the effect of the metal shield on the structures, 3D EM simulations have to be carried out. These simulations can take an enormous amount of time due to the very high mesh density caused by the dense narrow metal strips, and therefore slow down the design procedure significantly.

On the other hand, although being inferior to S-CPW in performance, microstrip lines are easier to model using EM simulators. Eliminating the substrate loss results in a G_d of zero (or almost zero), and EM simulation results for the rest of the line parameters R_d, L_d and C_d are relatively accurate. Moreover, one can simulate any passive structure such as capacitors and probe pads in a time efficient way in microstrip environment without employing special techniques (such as the shielded capacitor modeling method in [40]) as in S-CPW case. Last but not least, the modeling of the transistor is considerably simpler in microstrip environment. The modeling problems that can arise from a transistor access were highlighted in sections 3.4 and 3.5. Since there is no long ground leads connecting the transistor to side grounds, transistor modeling becomes much simpler in microstrip environment.

Considering the discussion above, we can conclude that designing mm-wave integrated circuits in microstrip environment is a safer option than in CPW environment, especially if first run success is aimed. In other words, if there is no chance to build test structures for characterization of the components before the actual design, microstrip designs are more likely to perform as expected; because the EM simulation modeling of the passive components is much more straightforward in microstrip designs. Because of this, microstrip environment is chosen to be used in the design of the amplifier presented in section 5. It is important to note, however, that the dielectrics in CMOS technologies are usually dispersive, and therefore predicting the actual characteristics of the passive structures at very high frequencies is difficult even in microstip designs.

4.3 Microstrip Line

Microstip lines are implemented using the top metal layer (M10) for the signal line, and the combination of the three bottommost metal layers (M1-M2-M3) for the ground layer. Thickness of M1-2-3 layers is one eighth of the thickness of the top metal layer, and therefore combining several metal layers for the ground helps

reducing the resistive losses. The distance between the signal line and ground plane is 3.6μm. Width of the signal line is set to be 7.2μm to obtain a characteristic impedance close to 50 Ω while keeping the resistive losses low. In order to fullfill the maximum metal density requirements, the three metal layers used in the ground plane are gridded and connected to each other with maximum possible density of vias.

If designed carefully, a gridded ground plane will behave like a Faraday cage and prevent electromagnetic field penetration into the substrate. The condition for a gridded ground plane to behave like a good Faraday cage is that the vertical distance between the signal and ground planes must be relatively higher than the dimensions of the gaps on the ground plane [39]. For example, if the maximum dimension of the gaps can be made 0.25μm, which is less than one tenth of the distance between the signal line and ground plane in our case, ground plane will act as a good Faraday cage. This is achievable in 28-nm FDSOI CMOS technology despite the strict metal density requirements. Figure 4.3.1 shows a unit cell of the ground plane used in this study. The dimension d is set to 0.25μm in order to obtain a good Faraday cage while fulfilling the maximum metal density and minimum space design rules. To further improve the structure, the three gridded metal layers used in the ground plane are placed on top of each other such that there is no opening to substrate is left. In this way, possible electromagnetic field penetration into the substrate is further prevented.

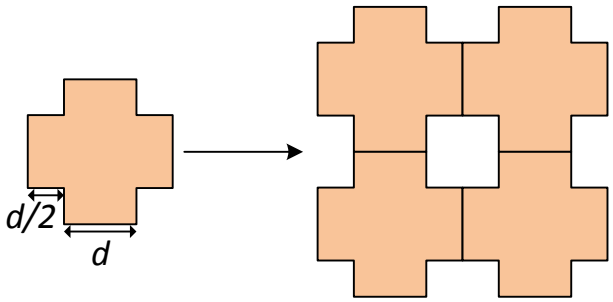


Figure 4.3.1: Ground plane grid

Due to minimum metal density requirements, dummy metal will be generated in between the signal and ground lines which will affect line characteristic significantly. It is not possible to predict the exact effect of dummy metals to the line, so it should be prevented. One way to solve this problem is adding ground planes on both sides of the microstrip line, similar to a CPW (Fig. 4.3.2). In this way, minimum metal density requirements can be fulfilled. If the distance between signal and ground lines H is kept relatively lower then the distance between the signal line and the side ground planes L, mode of propagation is as in a regular microstrip [41]. In this design, we have not used side grounds as it complicates the layout, especially when the lines are to be connected to a lumped component. Instead, exclusion layers are used to prevent dummy generation in close proximity of the lines.

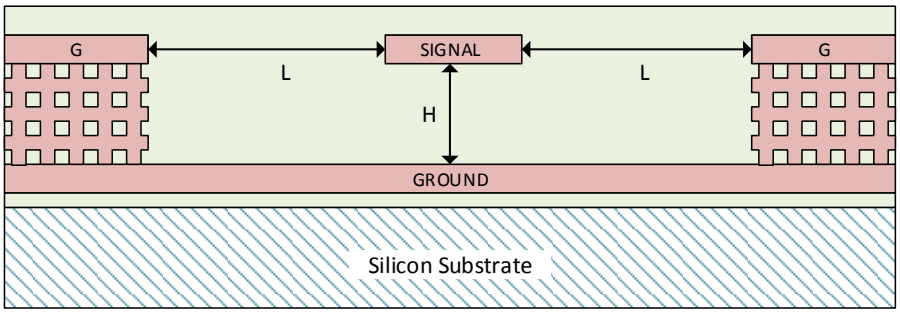


Figure 4.3.2: Simplified cross-section of the microstrip line with sidewalls

EM simulation is carried out for 200μm line section, then TLINP model parameters are optimized such that schematic simulation fits to the EM simulation results(Fig 4.3.3). Resultant model parameters are: Z=46 ohm, K=3.6, A=850 dB/m, F=34 GHz.

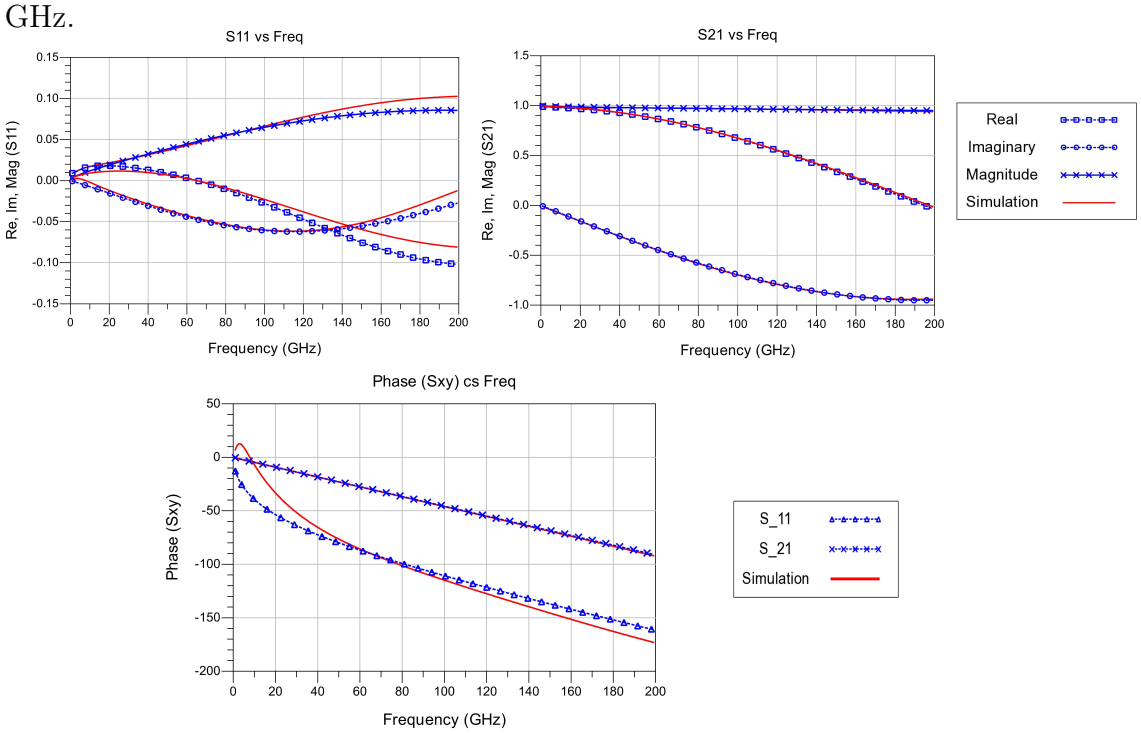


Figure 4.3.3: EM simulation vs. TLINP model S-parameters for the microstrip line

4.4 Capacitors

In mm-wave integrated circuits, the capacitive reactances needed in the matching networks are usually realized using transmission line sections. However, lumped capacitors are also needed for AC coupling and DC bypass which can not be done by transmission lines. Since these capacitors affect also the matching, optimizing their layout for better performance and modeling their behavior accurately at high frequencies are of great importance. Both AC coupling and DC bypass capacitors

should ideally have a zero impedance at the design frequency and infinite impedance at DC. Therefore, large, high quality factor capacitors with series self-resonance frequencies situated at the frequency of interest are desirable [42]. Even if the self resonant frequency is higher or lower then the design frequency, a capacitor can still work effectively if it has a sufficiently low impedance at the frequency of interest.

There are two main types of capacitor structures usually used in MMIC circuits: metal-oxide-metal (MOM) capacitors and metal-insulator-metal (MIM) capacitors. MOM capacitors are realized using the available metal layers and vias in the design kit. In order to increase the capacitance per area, they are designed using several narrow metal fingers in parallel. On the other hand, MIM capacitors generally requires 2 to 3 additional design layers, which naturally increases the number of required masks for fabrication and therefore increases the wafer cost. The advantage of the MIM capacitors is their high capacitance density. Since the insulator between the top and bottom plates of a MIM capacitor is very thin and has a high relative dielectric constant, this type of capacitors provide a considerably higher capacitance density than that of a MOM capacitor. Therefore, utilizing MIM capacitors for mass productions can even cost less as it saves a lot of area.

AC Coupling Capacitors Due to the reason that the circuit designed in this work is to be fabricated as prototype, using MIM capacitors do not change the cost of the chip. However, the EM simulation results of the MIM capacitors indicated that these capacitors present a significant resistive loss at high frequencies, mainly due to the high sheet resistivity of their top plate which is not actually a metal but a ceramic material. For this reason, custom designed multi-finger MOM capacitors are utilized in the design. Figure 4.4.1 shows the designed AC coupling capacitor. It is realized using the four top most metal layers, M7 to M10. In order to maximize the capacitance density, minimum allowed metal width and minimum metal spacing are used. M4, M5 and M6 layers are not utilized in the finger capacitor to reduce the parasitic capacitance between the MOM capacitor and ground plane which is at M3 layer. 2μm wide slabs composed of all four metal layers (M7-M10) are connected to each side of the capacitor so that the inductance between the ports and the different fingers of the capacitor is low. A small 45° taper is used to connect the slabs to the microstrip line.

Figure 4.4.2 shows the EM simulation results for the designed capacitor. It is seen that the self resonant frequency of the capacitor is situated at 110 GHz. In this way, the capacitor will present a lower impedance at the higher edge of the W-band, where the transistor has a lower gain than it has at lower frequencies in the W-band. Having the self resonance at such a point helps when a wide-band amplifier is to be designed as in our case.

DC Bypass Capacitors In the designed LNA circuit, which will be presented in section 5.3, bypass capacitors have two functionalities. They are either used to provide a good RF short circuit at the design frequency for shunt matching stubs and decouple the high impedance DC supply network, or to stabilize the transistors at lower frequencies by introducing resistance to their gates. Due to the reasons

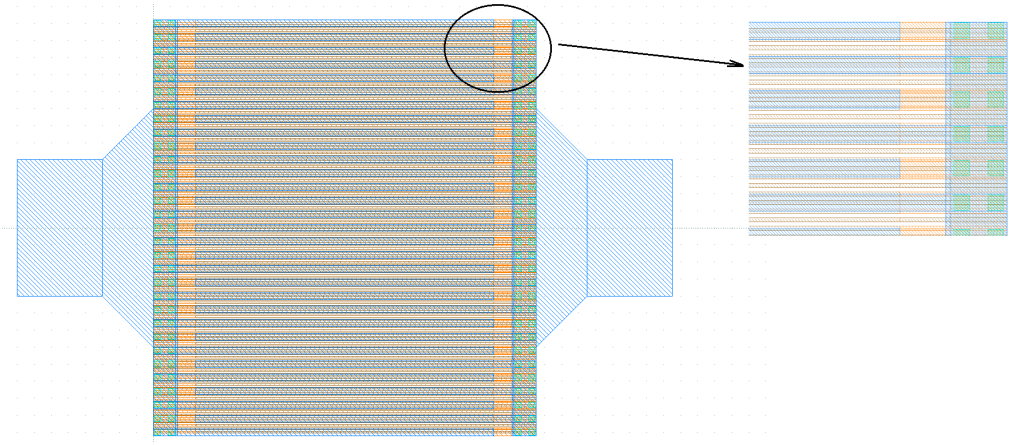


Figure 4.4.1: Top view of the AC coupling multi-finger MOM capacitor layout

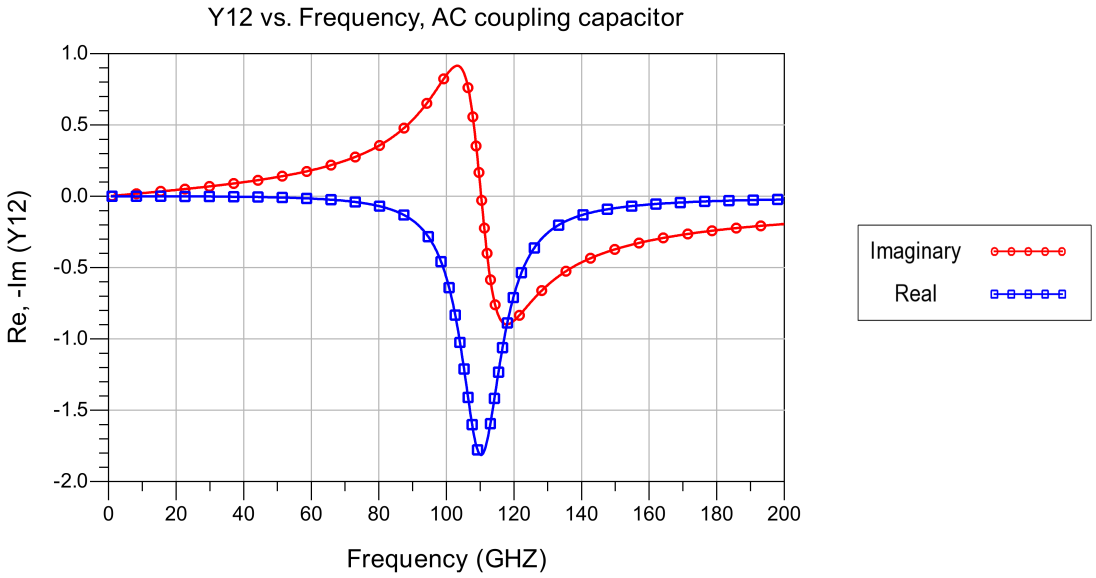


Figure 4.4.2: Y-parameters of the AC coupling MOM finger capacitor

explained in the previous section, custom designed multi-finger MOM capacitors are used as RF short-circuiting capacitors instead of MIM capacitors. On the other hand, MIM capacitors are utilized as low frequency stabilization capacitors as they do not appear in the RF path of the circuit, and therefore do not have to be low loss. Figure 4.4.3 shows the designed RF short-circuiting capacitor which consists of two MOM capacitor cells connected to a piece of transmission line. One port of each capacitor cell is connected to the the signal line, while their second ports are connected to the ground plane at the other end. The overall capacitor is designed to be a two port in order to be able to predict its behavior when a bias network is connected to its second port. It is realized using all the metal layers in between the ground and signal layers, M3 to M10. In order to maximize the capacitance density, minimum allowed metal width and minimum metal spacing are used.

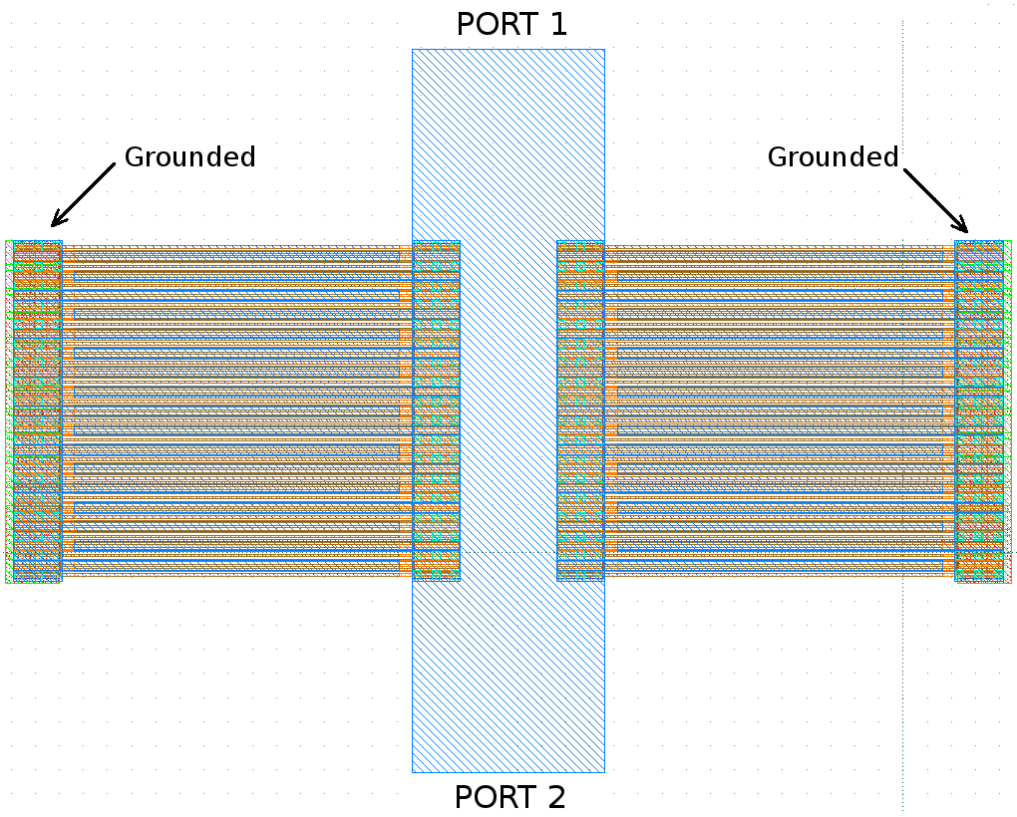


Figure 4.4.3: Top view of the RF short-circuiting multi-finger MOM capacitor layout

After the two-port EM simulation is completed, second port of the capacitor is connected to a high impedance load and it is simulated as a single port device in schematic window to analyze its resonance frequency. Figure 4.4.4 shows the simulation results for the designed bypass capacitor. It is seen that the self resonant frequency of the capacitor is situated close to 110 GHz as it was in the AC coupling capacitor. As explained before, having lower impedance at the higher edge of the frequency band of interest helps when a wide-band amplifier is to be designed.

4.5 Probe Pads

Usually, the probe pads are treated as part of the design, i.e. they are not de-embedded from the measurement results of amplifiers. Since they exhibit a relatively large capacitance between the signal path and ground, they affect the input and output matching networks considerably. Therefore, probe pads have to be modeled accurately after their layout is optimized to minimize the losses.

Figure 4.5.1 shows the designed GSG probe pad with a co-planar to microstrip transition. The center to center distance between the signal and ground pads is 100μm. In order to reduce the parasitic capacitance and resistive losses, signal pad size is kept as small as possible, 50μm; the lower limit is set by the measurement probe sizes. Corners of the signal pad are tapered to further reduce its effective size. As stated previously in section 3.2, a metal shield should be used under the probe

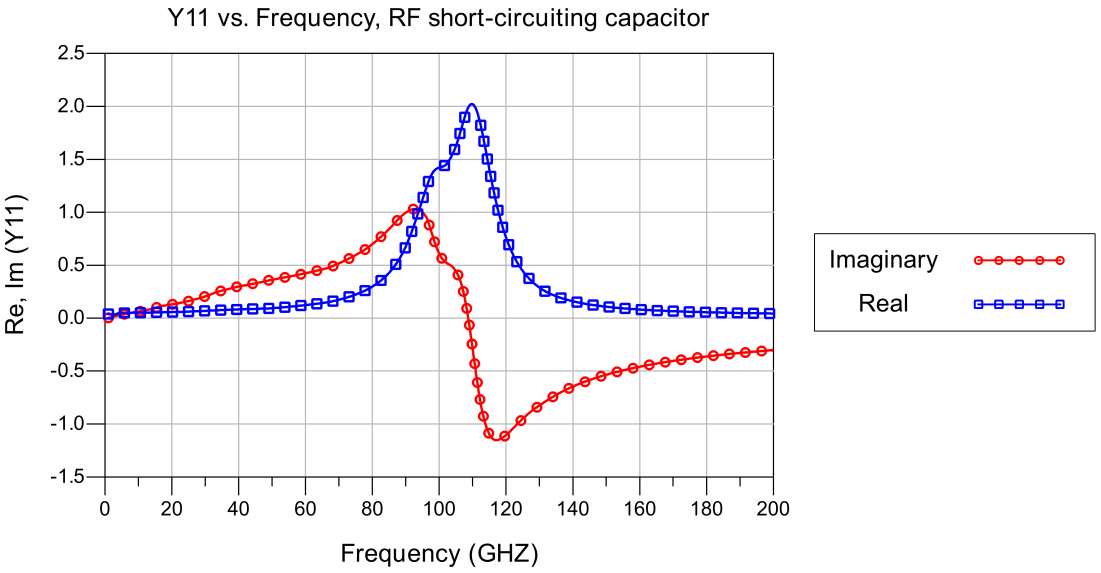


Figure 4.4.4: Y-parameters of the RF short-circuiting MOM finger capacitor

pads to prevent substrate losses. To this end, the ground plane is extended beneath the RF pads so that there is no opening left for EM waves to penetrate into the lossy substrate. Finally, ground pads are connected to the ground plane with maximum possible number of vias to reduce the losses.

Pad structure is simulated in Momentum as a 2-port and the resultant model is used in the design as a part of matching network.

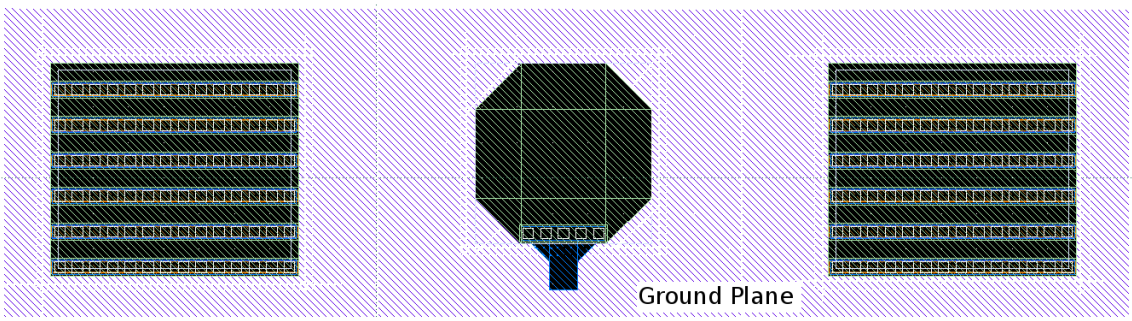


Figure 4.5.1: Top view of the shielded probe pad layout

4.6 Transistor Layout

Active device performance is strongly affected by the layout parasitics at mm-wave frequencies. In CMOS mm-wave design, it is possible to alter the device performance by changing the device layout in order to improve a particular performance metric in expense of other performance indicators.

Most important figures of merit for mm-wave devices are f_t, f_{max}, maximum stable gain at a given frequency and minimum noise figure. The unity current gain

frequency, f_t is equal to:

$$f_t = 2\pi \frac{g_m}{C_{gs} + C_{gd}} \tag{4.6.1}$$

where g_m is the transconductance, C_{gs} and C_{gd} are the gate to source and gate to drain capacitances of the device. As long as the layout is drawn in a reasonable way to not add extra capacitances, f_t mostly depends on the technology node, not on the layout [43]. On the other hand, f_{max}, unity unilateral power gain frequency, strongly depends on layout, and actually is a more appropriate metric to present the limit of the transistor. It is given as follows:

$$f_{max} = \frac{f_t}{2\sqrt{(R_g + R_s)(g_{ds} + 2\pi f_t C_{gd})}} \tag{4.6.2}$$

where R_g, R_s, g_{ds} are gate and source resistances and drain to source conductance respectively. In order to maximize f_{max}, one should minimize R_g, R_s and C_{gd}. Different transistor layout techniques are proposed in [37], [43], [44] and [45] to improve the f_{max} of the transistor.

The maximum stable gain (MSG) and maximum available gain (MAG) are other useful measures of device performance at a given frequency. MSG (or MAG) is a piecewise function of S_{21} and S_{12} depending on the value of stability factor K which will be discussed further in section 5.1.

$$MSG = \frac{|S_{21}|}{|S_{12}|} \qquad for \quad K \leq 1 \tag{4.6.3}$$

$$MAG = (K - \sqrt{K^2 - 1})\frac{|S_{21}|}{|S_{12}|} \qquad for \quad K > 1 \tag{4.6.4}$$

Above equations show how MSG and MAG are calculated. There is no point to define MSG for K>1 because in that region the device is unconditionally stable for any passive load, instead it is called MAG for K>1. Figure 4.6.1 shows the typical behavior of the maximum stable (or available) gain of a transistor as the frequency increases. Kink is observed at the point where the device becomes unconditionally stable (K=1 point).

It is important to note that the maximum gain and the maximum stable gain are two different metrics. A conditionally stable device can be used as an oscillator which has a power gain of infinity, and therefore maximum gain alone does not provide any meaningful information. For this reason, maximum stable gain is investigated.

Before the kink, where the device is conditionally stable, K is made equal to 1 (device is just in stable condition) by adding required loss, then the MSG is calculated [46]. Therefore, the internal gate and drain resistances of the transistor have no effect on the MSG at a certain frequency, as long as they are small enough that the device is still potentially unstable at that frequency [43]. However, an increase in the gate or drain resistance of the transistor shifts the kink to lower frequencies and decrease f_{max}. As a result, high frequency performance of the transistor degrades.

To analyze the relation between the transistor small signal parameters and the maximum stable gain, the MSG can also be expressed in terms of small signal

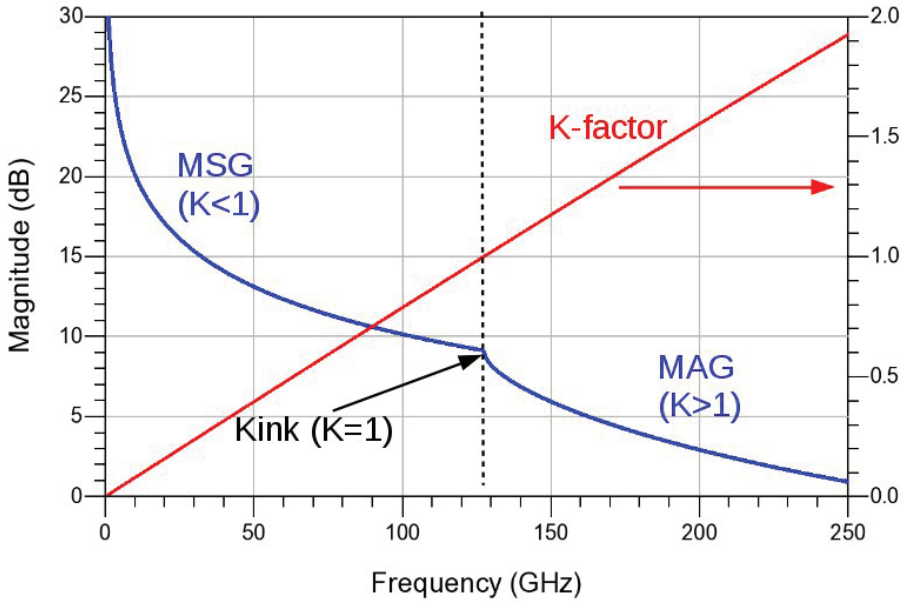


Figure 4.6.1: Typical behavior of maximum stable gain and stability factor of a transistor at mm-wave frequencies

parameters as follows,

$$MSG \approx \frac{g_m}{wC_{gd}} \tag{4.6.5}$$

So, g_m/C_{gd} ratio must be kept high to obtain high MSG. Relevant layout techniques are mentioned in [43].

As far as noise performance of the transistor is concerned, Fukui's equation helps us to understand which parasitics affect the minimum noise figure of the device [47]:

$$F_{min} = 1 + k_f w C_{gs} \sqrt{\frac{R_g + R_s}{g_m}} \tag{4.6.6}$$

where k_f is and empirical fitting factor. Due to the reason that in CMOS technology transistor gates are implemented using polysilicon, which has a significantly larger resistivity than copper, R_g is usually the dominant term in this equation.

To be able to build transistors of various sizes with high performance, layout of a unit cell transistor is optimized. Two or more of these unit cells can be connected together to form larger size transistors without a significant drop in high frequency performance. Figures 4.6.2 and 4.6.3 show simplified versions of the optimized layout of a unit cell transistor and a complete transistor layout made of this unit cell respectively. In order to reduce the gate resistance, finger width is kept at 0.9 μm and the gates are connected to M1 layer on both sides of each finger. Similarly, double sided source connection is realized using M3 layer to reduce source resistance while keeping gate to source capacitance low. Connection of the drain port to the fingers is done from above the fingers using M6 layer, so that both gate to drain and drain to source capacitances remain low. The number of fingers in the unit cell is kept small in order not to end up with a long gate connection, which will increase

the gate resistance. The gain and noise performance of the designed transistor at different bias points will be presented in section 5.4.

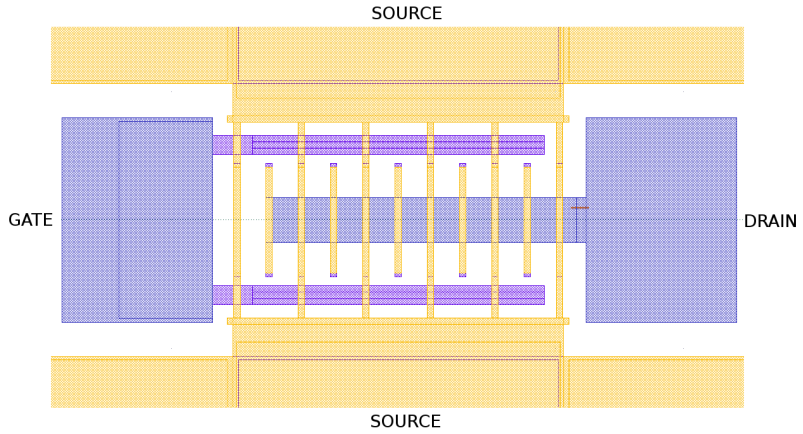


Figure 4.6.2: Simplified layout of the unit cell transistor

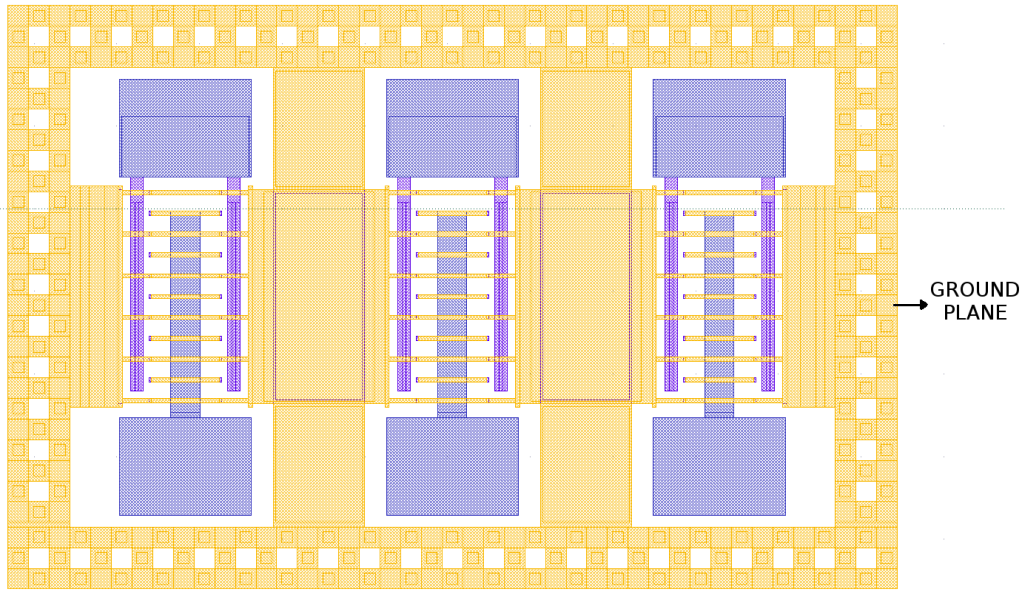


Figure 4.6.3: Simplified layout of the complete transistor

5 Millimeter-Wave Low-Noise Amplifier Design

Amplifiers are critical building blocks in communication systems. As the first block in the receiver, a low-noise amplifier is needed to amplify the received signal and suppress the noise effect of the subsequent stages. Power amplifiers are essential in the transmitter part of the system as they convey the modulated data to the antenna.

In this section, basic considerations related to design of CMOS low-noise amplifiers, such as gain, noise figure, stability, linearity and power consumption, are discussed. Finally, a full W-band amplifier with the following design specifications is designed:

- Flat gain of at least 15 dB over whole W-band (75-110 GHz).
- Input and output return losses greater than 10 dB (S_{11} and S_{22} less than -10 dB)
- Noise figure less than 6 dB
- Power consumption less than 50 mW
- Output 1 dB compression point (OCP_{1dB}) higher than 0 dBm.

5.1 Stability Analysis

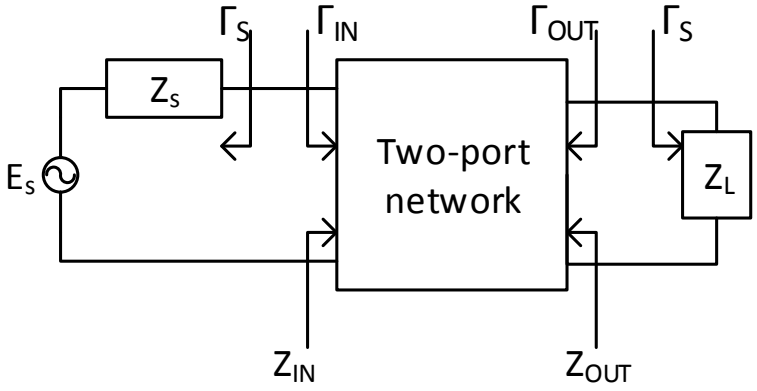


Figure 5.1.1: Two port network and important parameters used in stability analysis

One of, if not the most critical considerations in amplifier design is the stability. Unless enough care is taken, an amplifier can turn into an oscillator. Stability of an amplifier can be determined from the S-parameters, terminations and the matching networks. Two port network shown in Figure 5.1.1 can be used for stability analysis. Such a two port network is called to be unconditionally stable if the following conditions are satisfied.

$$|\Gamma_S| < 1 \tag{5.1.1}$$

$$|\Gamma_L| < 1 \tag{5.1.2}$$

$$|\Gamma_{IN}| = |S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}| < 1 \tag{5.1.3}$$

$$|\Gamma_{OUT}| = |S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}| < 1 \tag{5.1.4}$$

Violation of any of these conditions is equivalent to have a negative resistance presented in the circuit which will lead to possible oscillations. Equations 5.1.1 and 5.1.2 indicates that the source and load are passive, while 5.1.3 and 5.1.4 indicate that input and output impedance must also be passive. An easier way to check these conditions is using stability circles which are great graphical tools for this job. As

Γ_{IN} and Γ_{OUT} are functions of load and source impedances, regions where Γ_L and Γ_S produce $|\Gamma_{IN}| < 1$ and $|\Gamma_{OUT}| < 1$ are drawn on Γ_L and Γ_S planes. Figures 5.1.2 and 5.1.3 summarizes the stable and unstable regions for Γ_L and Γ_S.

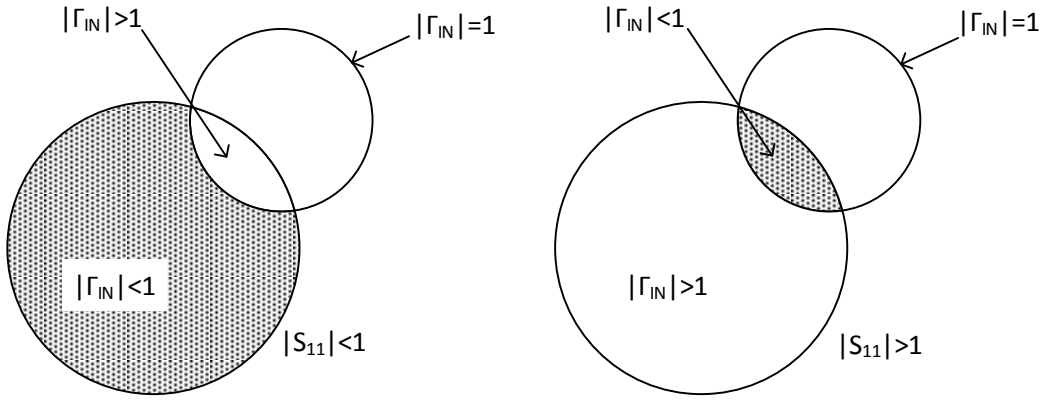


Figure 5.1.2: Illustration of stable and unstable regions in the Γ_L plane

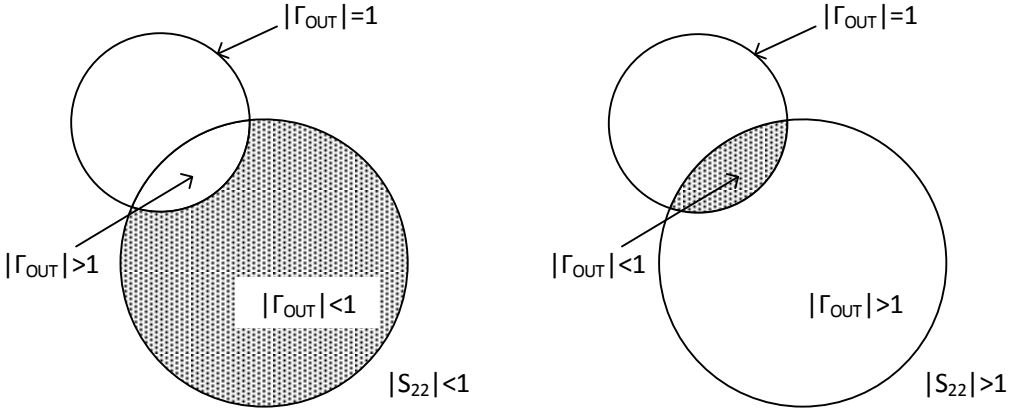


Figure 5.1.3: Illustration of stable and unstable regions in the Γ_S plane (Dotted regions are stable)

As long as the source and load are passive, i.e $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$, it is also possible to derive necessary and sufficient conditions for a two port to be unconditionally stable by manipulating equations from 5.1.1 to 5.1.4. These conditions, which we will call k-factor conditions, are

$$K > 1 \tag{5.1.5}$$

$$|\Delta| < 1 \tag{5.1.6}$$

or

$$K > 1 \tag{5.1.7}$$

$$B > 0 \tag{5.1.8}$$

where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{5.1.9}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{5.1.10}$$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{5.1.11}$$

K, Δ and B are stability factor, delta and stability measure respectively. Usually, RF design tools, such as ADS, provide ready functions for these parameters to speed up the design procedure.

It is very important to note that k-factor analysis is applicable only to a single stage amplifier. In a multistage amplifier, the conditions $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$ no longer apply, because the input and/or output planes of an intermediate stage are terminated with active networks [48]. There are mainly two ways to ensure that a multistage amplifier is stable. First, one can carry out the k-factor analysis for each stage of the amplifier, as well as for the whole cascade. If all off them satisfy the k-factor conditions, then the amplifier is stable. However, this is a sufficient but not necessary condition, and if an amplifier is designed in this way, it is very likely to get a poor gain performance. To avoid this problem, one can use the stability test proposed in [49] which is based on Nyquist stability criterion. A more detailed explanation of theory behind this technique can be found in [50].

For a potentially unstable device, which is usually the case at the frequency of operation, there is a trade-off between the gain and stability. For lower gain values, matching networks can be designed to keep the source reflection coefficient further from the stability circles to ensure stability. One can also add extra resistance to the input or output of the transistor to move the stability circles outside the unit circle to ensure stability. However, this will reduce the gain and increase the noise.

5.2 Noise Figure and Linearity of a Multistage Amplifier

In this section, some basic relationships between gain, noise figure and linearity of multistage amplifiers will be reviewed.

Noise Figure Noise factor (F) is the measure of degradation of the signal-to-noise ratio (SNR), and it is defined as:

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{5.2.1}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios at the input and output. And the noise figure (NF) is defined as the noise factor in dB:

$$NF = 10log(F) \tag{5.2.2}$$

Friis formula gives the total noise factor of a cascade in terms of the noise factor and gain values of individual stages in the cascade [51]. It can be written as:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{5.2.3}$$

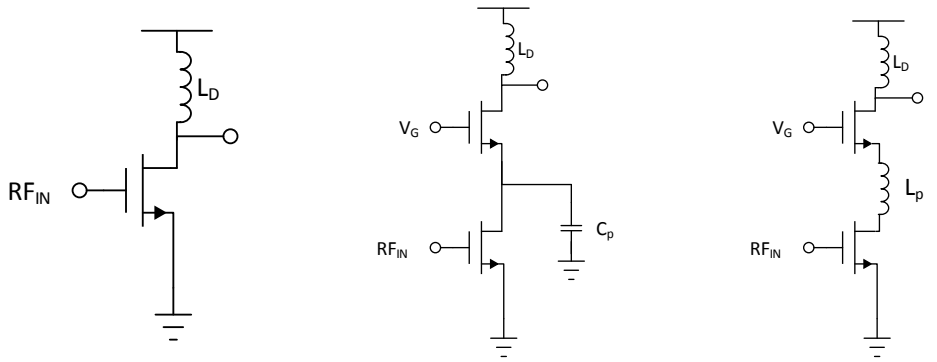
where F_i and G_i are the noise factors and available power gains, respectively, of individual stages in the cascade. Hence, the gain of the first stage should be high to minimize the total noise figure of the amplifier.

Linearity Linearity is usually quantified in terms of 1-dB compression point or third-order intercept point (IP3). The total IP3 of a cascade can be expressed as follows [52]:

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + ... \tag{5.2.4}$$

where $IIP3_i$ and G_i are the input-referred IP3 (in watts) and the power gains (in watts/watts), respectively, of each individual stage of the amplifier. According to this equation, linearity of the latter stages will dominate the overall linearity. Therefore, to maximize the linearity of the overall amplifier, the linearity of the output stage should be maximized.

5.3 Amplifier topology



(a) (b) (c)

Figure 5.3.1: Common mm-wave CMOS amplifier topologies: (a) common-source, (b) cascode, (c) cascode with an inductor at the shared junction

Two of the most common topologies in mm-wave CMOS amplifiers are cascode and common source topologies (Figure 5.3.1). The cascode topology provides high gain, good stability and low power consumption [41]. In addition, it is nearly unilateral so that it gives a good reverse isolation, and therefore matching becomes simpler [42]. Regular cascode transistors, however, have a large parasitic capacitance on the

shared junction node, between two transistors (C_p in Figure 5.3.1b). This capacitance presents a low impedance at high frequencies and reduces the gain of the cascode structure. It is possible to resonate out the capacitance at the interstage node by placing a series inductor between the devices as shown in Figure 5.3.1c. However, this can complicate the modeling of the cascode structure. On the other hand, common source (CS) topology provides higher output voltage and current swings at the output, and does not suffer from an interstage parasitic capacitance. Last but not least, when operating close to cut off frequency, noise figure of a common source is relatively low compared to that of a cascode. This is because the noise performance of the cascode structure degrades due of the reduced degeneration on the cascode device at high frequencies[53].

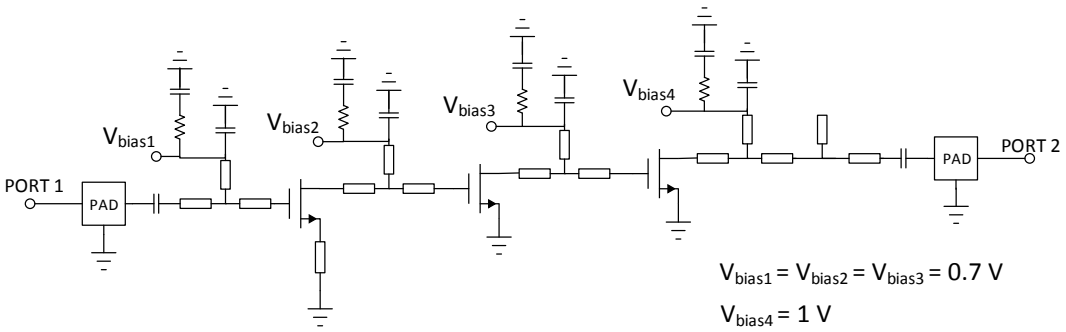


Figure 5.3.2: Simplified schematic of the three stage W-band LNA

In this study, three stage common source topology is used to design the W-band amplifier mainly due to its superior noise features. Simplified schematic of the amplifier is given in Figure 5.3.2. For the input and inter-stage matching network, transmission line section in series and short circuited shunt stub forms are used. For the output matching network, an open circuited shunt stub is utilized in addition to the series lines and a short circuited shunt stub in order to obtain a wideband matching. The widths of the transistors in the first two stages are equal to 27 μm, while the output transistor width is chosen to be twice as big, 54 μm. In this way, the current swing at the output stage is increased, and therefore linearity of the amplifier is improved. Large MIM capacitors in series with 20 Ω resistors are connected to the RF short circuit nodes of the circuit in order to ensure stability at low frequencies. To minimize the number of AC coupling capacitors, which can easily alter the overall response of the amplifier in case of a slight modeling error, gate and drain of the transistors in the first two stages are biased to the same voltage, while the drain voltage of the output transistor is set to a higher voltage to improve linearity. Detailed explanation of the bias point selection is presented in the next chapter.

In order to improve the noise performance, a series feedback is applied by a section of transmission line connected between the source of the input transistor and ground. In this way, source impedance required for optimum noise match gets closer to the source impedance required for the maximum gain match [42].

5.4 Selection of Bias Points for Improved Gain, Noise Figure and Linearity

By careful selection of the bias points of the transistors, it is possible to obtain better gain, noise and linearity performance at mm-wave frequencies. To ensure that the transistors are in saturation and to improve linearity of small-signal amplification, V_{ds} of the transistors should be high. However, maximum possible V_{ds} is limited by the technology rules and equal to 1 V in 28-nm FDSOI CMOS technology .

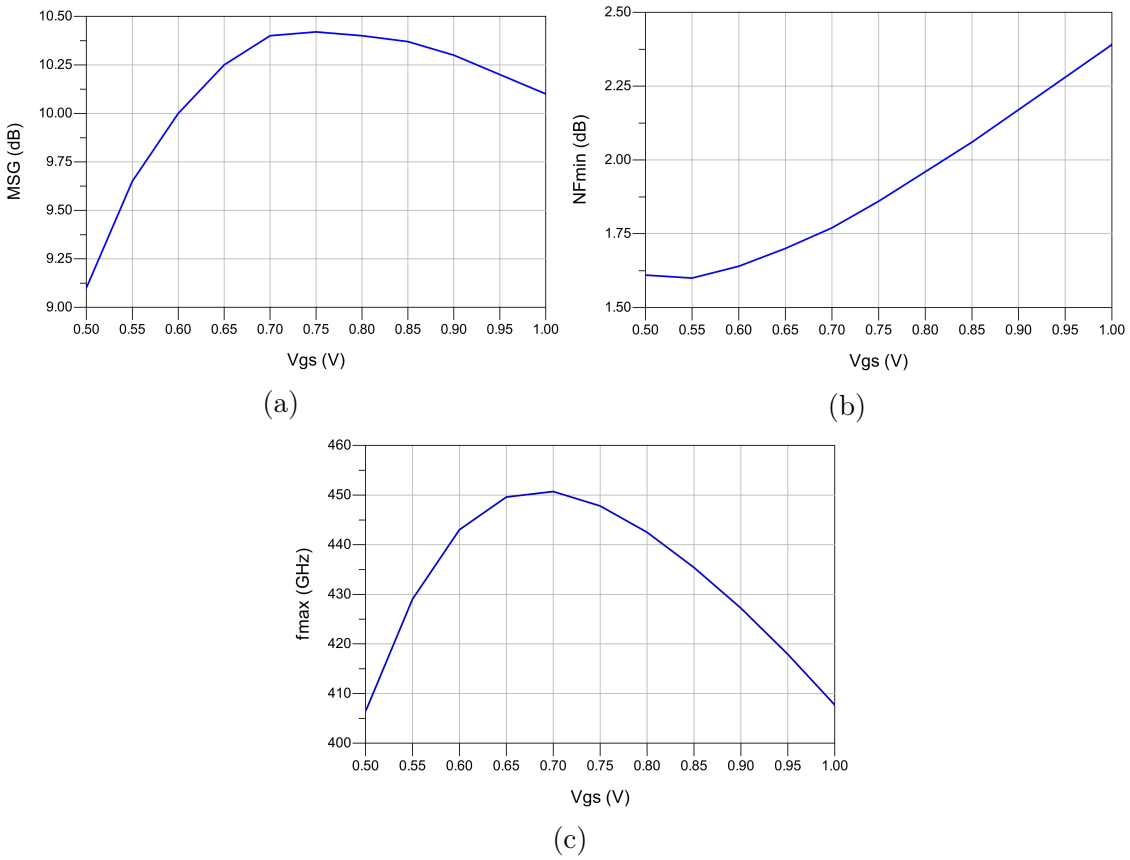


Figure 5.4.1: Change of (a) MSG (@ 90 GHz), (b) NF_{min} (@ 90 GHz), and (c) f_{max} with V_{gs} for a single transistor in common source configuration where V_{ds}=1 V.

Figure 5.4.1 shows the change of MSG, NF_{min} and f_{max} with V_{gs} for a single transistor in common source configuration where V_{ds} is equal to 1 V. MSG and NF_{min} are plotted for 90 GHz, but the shapes of these graphs remain the same also at other frequencies. It is seen that the maximum gain is obtained when V_{gs} is 0.75 V, while the minimum noise figure is obtained when V_{gs} is 0.55 V. To make a conclusion about the linearity, we should examine the f_{max} plot. In the region where f_{max} is flatter, which is between V_{gs}=0.65 V and V_{gs}=0.75 V, transistor behavior is more linear [54]. Considering all these, V_{gs}=0.7 V and V_{ds}=1 V are chosen as the gate and drain bias voltages for the output stage to obtain high gain, low-noise figure and good linearity. Although the NF_{min} is slightly higher than its minimum value at

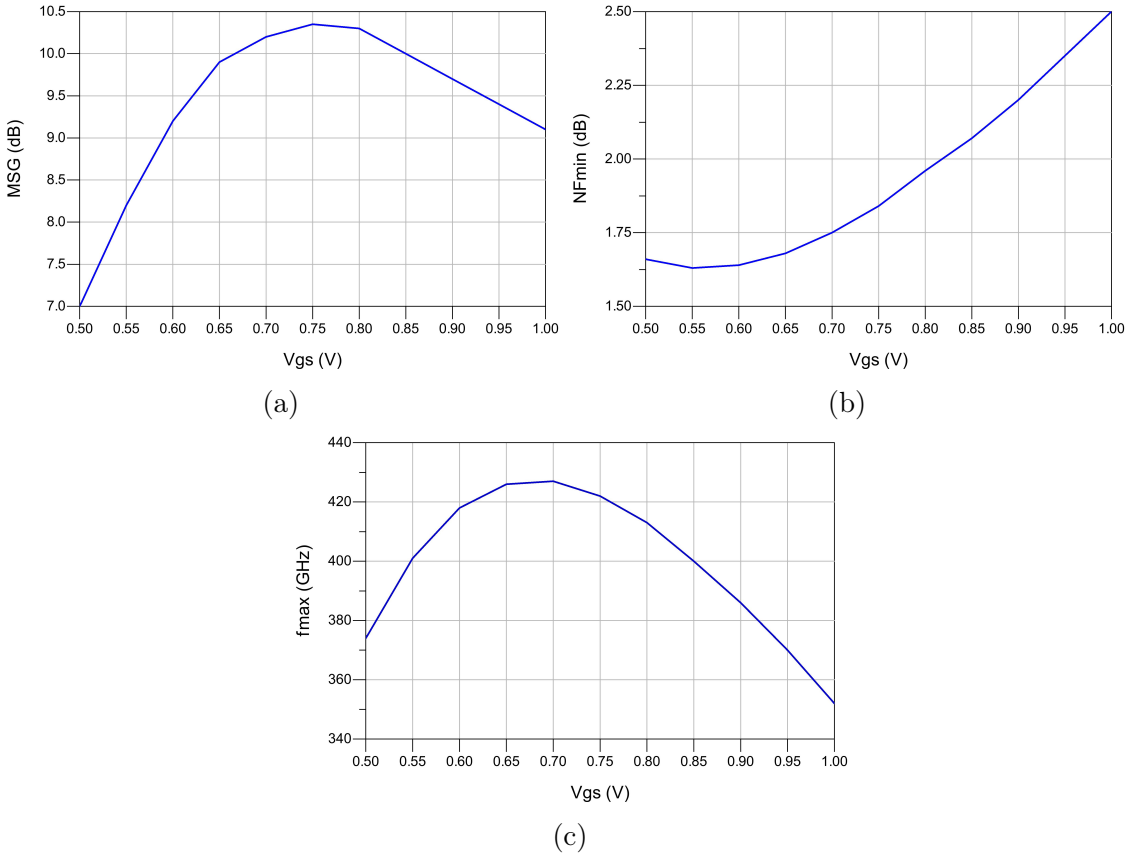


Figure 5.4.2: Change of (a) MSG (@ 90 GHz), (b) NF_{min} (@ 90 GHz), and (c) f_{max} with V_{gs} for a single transistor in common source configuration where V_{ds}=0.7 V.

this bias point, the overall noise performance of the transistor would not change that much as the gain is also higher at V_{gs}=0.7 V.

As stated in the previous section, gates and drains of the transistors in the first two stages are biased to the same voltage in order to avoid usage of additional AC coupling capacitors. Therefore, both V_{gs} and V_{ds} are set to 0.7 V for the first two stages. Although the drain bias voltage is lower than the optimum one, noise and gain performances of the transistors are not affected remarkably. Figure 5.4.2 shows the change of MSG, NF_{min} and f_{max} with V_{gs} for a single transistor in common source configuration where V_{ds} is equal to 0.7 V. When compared to Figure 5.4.1, it is seen that the gain and noise figure performances at the bias point V_{gs}=0.7 V, V_{ds} =0.7 V are close to the ones at V_{gs}=0.7 V, V_{ds} =1 V. Only the linearity would comparatively degrade, since the voltage swing at the output of a transistor is reduced for a lower drain voltage. This, however, would not affect the overall linearity of the amplifier that much, since it is dominated by the linearity of the last stage which uses a drain voltage of 1 V.

5.5 Input-matching principle

An effective way of designing the matching network is using the available gain, noise and source stability circles of the input transistor drawn on a Smith chart. Figure 5.5.1 summarizes the matching principle of the input stage. As a first order approximation, the inter-stage matching circuits are also designed in a similar way. Afterwards, transmission line lengths are tuned in order to obtain a flat gain and noise figure response over a wide-band while keeping the reflections at the input and output below -10 dB.

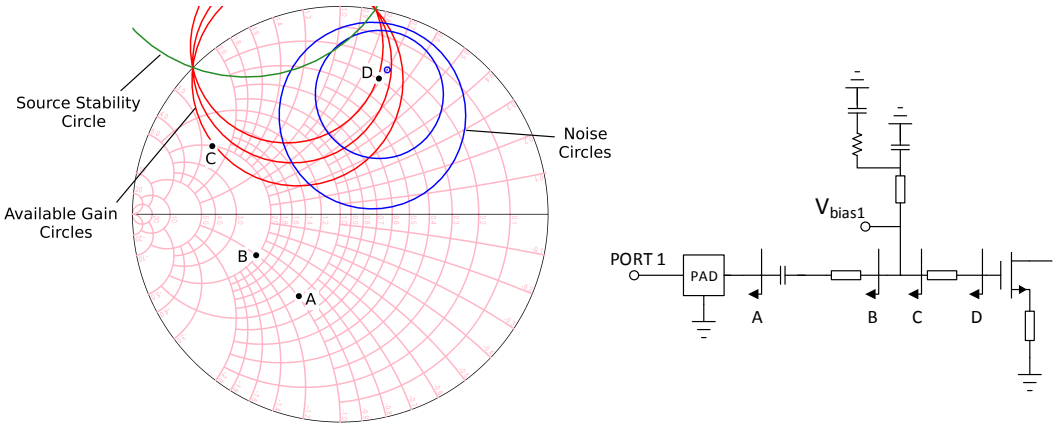


Figure 5.5.1: Input matching principle of the W-band low noise amplifier. Impedance after each matching component is plotted on the Smith chart. Source stability circle, avaliable gain circles and noise circles of the 27 μm sized transistor are plotted at 100 GHz.

5.6 Simulation Results

Figure 5.6.1 shows the simulated S-parameters of the designed W-band amplifier. The amplifier has a flat gain of 15 dB between 60 to 115 GHz with a maximum deviation of 1.3%. Both input and output return losses are greater than 13 dB between 75-110 GHz and the simulated reverse isolation (S_{12}) is less than -38 dB over the whole frequency range (not shown).

The simulated stability factor and stability measure are shown in Figure 5.6.2. They are above one and zero, respectively, which is a necessary condition for stability of the amplifier. The simulated source and load stability circles are shown in Figure 5.6.3. All the circles are outside the unit circle (Γ=1) also indicating that the amplifier is stable. In order to ensure the stability of inter-stage nodes of the amplifier, stability test proposed in [49] has also been carried out, and it is verified that there is no oscillation at any node of the circuit.

Figure 5.6.4 shows the simulated noise figure of the amplifier. It is seen that the noise figure is below 6 dB between 75-110 GHz and it is relatively flat over this range.

The simulated output 1-dB compression and output saturation points are shown in Figure 5.6.5. It is seen that the amplifier achieves an output 1-dB compression point of 3.5 dBm and an output saturation point of 8.2 dBm at 95 GHz. The variation of both points are in a reasonable range over the W-band.

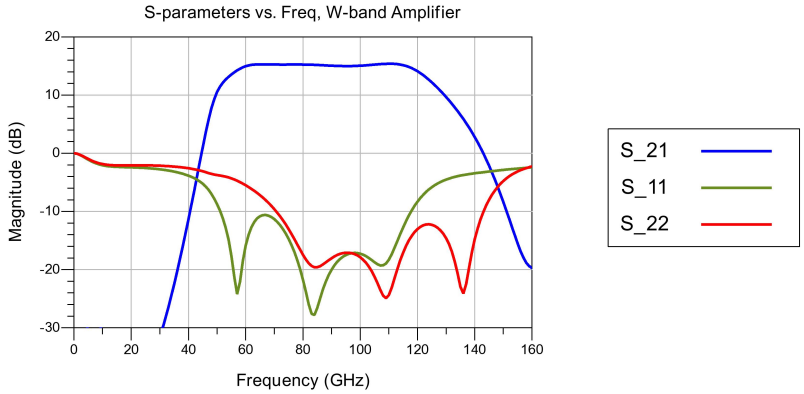


Figure 5.6.1: Simulated S-parameters of the W-band amplifier

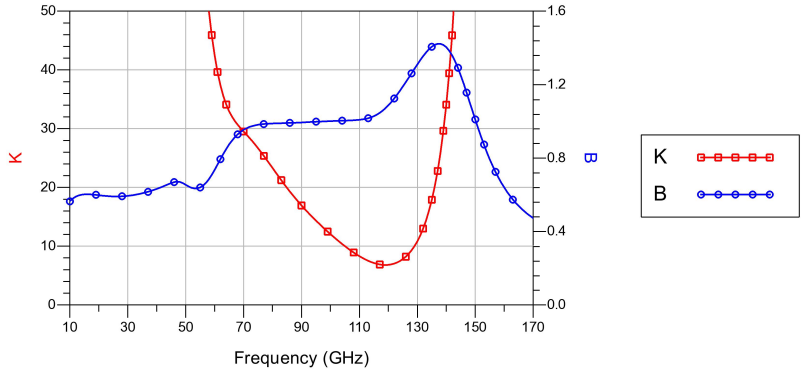


Figure 5.6.2: Simulated stability factor and stability measure

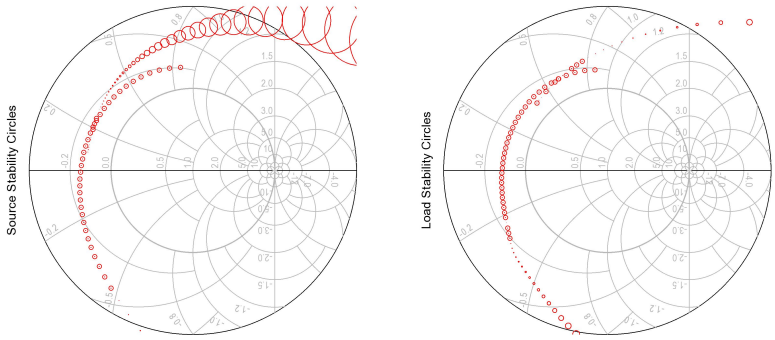


Figure 5.6.3: Simulated source and load stability circles

The simulated total power consumption of the 3-stage amplifier is 38.2 mW. In detail, the transistors in the first two stages consume 10.3 mA each from a 0.7 V supply, while the output stage transistor consumes 23.8 mA from a 1 V supply.

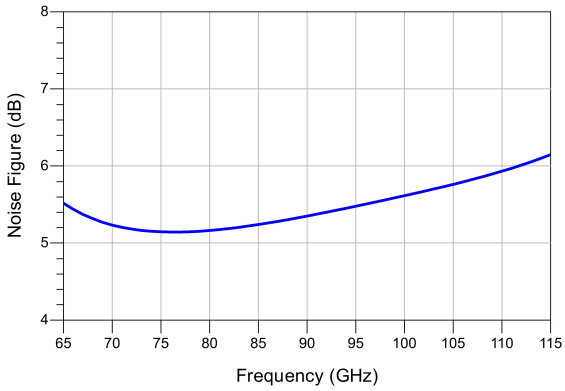


Figure 5.6.4: Simulated noise figure of the W-band amplifier

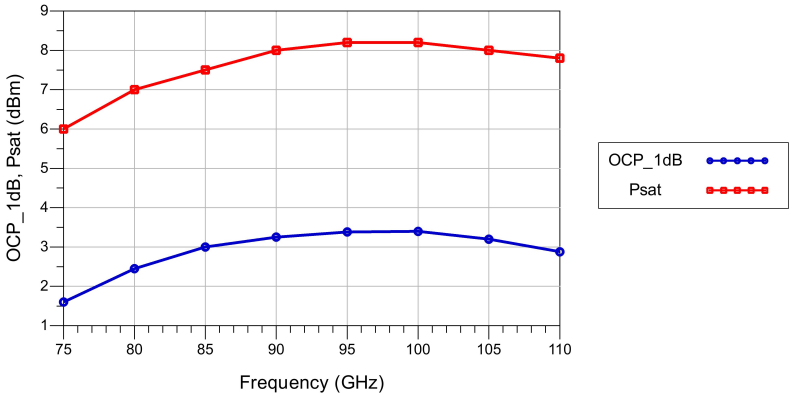


Figure 5.6.5: Simulated output 1-dB compression and output saturation points versus frequency

5.7 Layout of the W-band LNA

Layout of the designed 3-stage W-band LNA is shown in Figure 5.8.1. The total size of the amplifier layout is 1.15 x 0.41 mm^2. By using meander type structures for the long transmission line sections, it is possible to further reduce the size of the layout. However, in order to make the circuit bond-wire compatible, the signal pads have to be placed at the edges of the chip so that the effect of the parasitic inductances of the bond-wires on the circuit performance is minimized. For this reason, the width of the circuit is intentionally adjusted to 1.15 mm, which is determined by the rest of the circuits on the same chip.

5.8 Comparison of the W-band LNA with the Previous Works

The simulated performance and the layout size of the W-band LNA is compared with previously published results in Table 3. As can be seen, the three-stage common-source amplifier designed in this work achieves a very low noise figure and a reasonable gain, and it has the widest bandwidth among all. The area of the amplifier is relatively large compared to the others due to the reason that microstrip lines are utilized in

the design instead of slow-wave CPWs. The 1-dB output compression point and the saturated output power of the designed amplifier is considerably high compared to most of the other works.

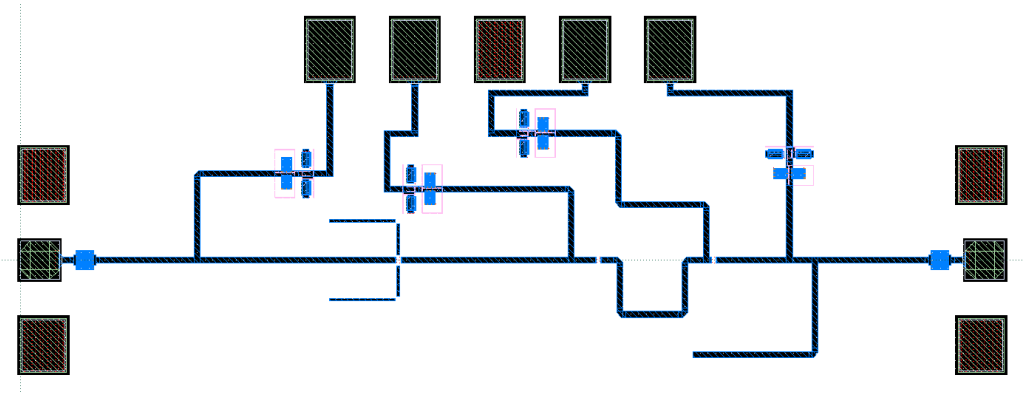


Figure 5.8.1: Layout of the 3-stage W-band LNA

Table 3: Performance comparison of CMOS W-band amplifiers

CMOS process	**Freq. (3-dB BW) [GHz]**	**Gain [dB]**	**NF [dB]**	**Area [mm^2]**	**OCP$_{1dB}$ [dBm]**	**P$_{sat}$ [dBm]**	**P$_{dc}$ [mW]**	**Topology**	**Ref**
90-nm Bulk	77-81	13	6.2	0.6	-20	-11	21.1	3-stage CS	[55]
65-nm Bulk	100-118	25	7	0.25	-6	-3	48	4-stage cascode	[56]
65-nm Bulk	83-93	27	7	0.4	-	-	30	5-stage cascode	[57]
65-nm Bulk	72-92	13.5	6.4	-	-	4	33	3-stage cascode	[58]
45-nm SOI*	89-107	10.7	6	0.32	5	7.5	52	3-stage CS	[1]
45-nm SOI	76-88	13.5	5.7	-	-1.5	-	13.5	3-stage CS	[45]
28-nm Bulk	91-91.2	32	5.3	0.28	-12.8	-	36	6-stage cascode	[59]
28-nm FDSOI**	58-122	15	5.5***	0.47	3.5	8.2	38.2	3-stage CS	[This Work]

* SOI: Silicon on Insulator
** FDSOI: Full Depleted SOI
*** at 80 GHZ

6 Conclusion

Thanks to the downscaling of the technology nodes, CMOS has become an alternative to III-V semiconductor technologies for mm-wave designs. Consequently, there has been a tremendous interest in CMOS mm-wave circuits in recent years. Accurate characterization and modeling of the devices is a key aspect in design of CMOS mm-wave integrated circuits. In this thesis, characterization of active and passive MMIC components via different de-embedding techniques, modeling of passive structures with lumped circuit components and design of mm-wave small signal amplifiers in CMOS technology have been studied.

Modeling of passive and active devices has an increasingly critical role in mm-wave designs since skin effect, proximity effects and substrate losses are involved at high frequencies. Such high frequency effects also complicate the characterization of on-chip components. Possible difficulties that can be come across with in mm-wave device characterization have been discussed. Several de-embedding techniques have been analyzed and compared to offer an insight into their strengths and weaknesses, and ultimately to provide useful information about how to overcome the aforementioned challenges. Much characterization work has been performed on on-chip pads, lines and transistors. It has been shown that the access used to connect a transistor to the CPW-lines can have a significant effect on the device performance. This effect has been examined in detail and its impact on accuracies of various de-embedding methods has been investigated with simulations. A new de-embedding method has been proposed for characterization of the DUT and DUT access. It has been demonstrated that the proposed technique is an effective tool to characterize the transistor access at least up to 110 GHz.

On-wafer active and passive component characterization work carried out in section 3 of this thesis has played an important role in publication of three conference papers [60][61][62] which are accepted to European Microwave Integrated Circuits conference. The new de-embedding technique proposed in section 2.5 will be submitted as a long journal article [34].

It has been shown that the post-layout design kit model of a transistor in strong inversion is accurate up to W-band frequencies in 28-nm node. After careful modeling of the passives, designers can focus on the circuit performance trusting the design kit models for the actives. However, it would be wise to carry out a more detailed study to investigate the accuracies of the 28-nm design kit models for different bias points in different operation modes before making a final conclusion.

Advantages and disadvantages of using coplanar waveguide, shielded coplanar waveguide or microstrip line have been presented. The effects of their geometry and ground plane configuration have been discussed. It has been concluded that if substrate losses are involved, electromagnetic simulators might fail to model the passives accurately, and therefore test structures are required for characterization. However, as long as the substrate losses are eliminated as in microstrip environment, EM simulations can give accurate enough results for mm-wave designs. In such cases, accuracy of the simulations are dependent on the loss tangents and dispersive properties of the dielectrics appearing in that particular technology. Further study

can be carried out to analyze such properties of the dielectrics in 28-nm CMOS technology in order to make more detailed conclusions about the accuracy of EM simulations in microstrip environment for this technology. Moreover, provided that there are sufficient number of test structures to analyze, one can replace the dielectric stack by a single effective dielectric layer that reflects the frequency dependent properties of the whole stack as done in [31]. Findings from such a study would be very useful for future designs, since it would enable the designers to model all the passives with the help of EM simulations.

A W-band low-noise amplifier, which is designed in microstrip environment to avoid modeling problems encountered in CPW environment, has been presented. Design and modeling of active and passive structures used in the LNA have been explained in detail. Extensive stability analysis has been carried out. The amplifier achieves a gain of 15 dB and a noise figure of less than 6 dB over the whole W-band in the simulations. The power consumption of the LNA is 38.2 mW, and it has an output 1-dB compression of greater than 1 dBm in W-band. Layout size of the amplifier is 1.15 x 0.41 mm^2. Compared to the previous works in W-band, the designed amplifier has the widest bandwidth, it achieves a very low noise figure and a reasonable gain, it has a comparable power consumption and it has a considerably higher output 1-dB compression point than most of the others. Due to the reason that it is a microstrip design, the amplifier layout size is relatively large compared to the previous works.

The achieved results are promising and they indicate that the 28-nm CMOS technology can be utilized to build mm-wave circuits such as low-noise and power amplifiers, mixers, etc. operating above 100 GHz.

References

[1] B. Cetinoneri, Y. Atesal, A. Fung, and G. Rebeiz, "W-band amplifiers with 6-dB noise figure and milliwatt-level 170–200-GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 692–701, Mar. 2012.

[2] S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Gordon, G. Xiang, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, and C. H. Doan, "A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 164-166.

[3] L. Zhou, C. C. Wang, Z. Chen, and P. Heydari, "A W-band CMOS Receiver Chipset for Millimeter-Wave Radiometer Systems," *IEEE J. Solid State Circuits*, vol. 46, no. 2, pp. 378-391, Feb 2011.

[4] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A Passive W-Band Imaging Receiver in 65-nm Bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1981-1991, Oct 2010.

[5] B. Razavi, "A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider," *IEEE J. Solid-State Circuits*, vol. 43, pp. 477–485, Feb. 2008.

[6] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A highly integrated 60 GHz CMOS frond-end receiver," in *IEEE ISSCC Dig. Tech. Papers*, pp. 190–191, Feb. 2007.

[7] A. Parsa and B. Razavi, "A 60 GHz CMOS receiver using a 30 GHz LO," *IEEE ISSCC Dig. Tech. Papers*, pp. 190–191, Feb. 2008.

[8] A. Cathelin, B. Martineau, N. Seller, S. Douyere, J. Gorisse, S. Pruvost, C. Raynaud, F. Gianesello, S. Montusclat, S. P. Voinigescu, A. M. Niknejad, D. Belot, and J. P. Schoellkopf, "Design for millimeter-wave applications in silicon technologies," in *Proc. 33rd Eur. Solid State Circuits Conf.*, Munich, Germany, Sep. 11–13, 2007, pp. 464–471.

[9] S. Franssila "Economics of Microfabrication," in *Introduction to Microfabrication*, 2nd ed., Chichester, United Kingdom: John Wiley, 2010, pp. 458.

[10] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high frequency characterization," in *Proc. BCTM 1991*, pp. 188–191.

[11] L. F. Tiemeijer, and R. J. Havens, "A calibrated lumped-element de-embedding technique for on-wafer RF characterization of high-quality inductors and high-speed transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, Mar. 2003, pp. 823-829.

[12] R. Torres-Torres, R. Murphy-Arteaga, and J. A. Reynoso-Hernandez, "Analytical model and parameter extraction to account for the pad parasitics in RF-CMOS," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1335–1342, Jul. 2005.

[13] E. P. Vandamme, D. M. M.-P. Schreurs, and C. van Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 737–742, Apr. 2001.

[14] H. Cho and D. Burk, "A three-step method for the de-embedding of high-frequency S-parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1370–1375, Jun. 1991.

[15] T. E. Kolding, "A four-step method for de-embedding gigahertz on-wafer CMOS measurements," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 734–740, Apr. 2000.

[16] C. Andrei, D. Gloria, F. Danneville, and G. Dambrine, "Efficient de- embedding technique for 110-GHz deep-channel-MOSFET characterization," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 4, pp. 301–303, Apr. 2007.

[17] A. Issaoun, Y. Z. Xiong, J. Shi, J. Brinkhoff, and F. Lin, "On the de-embedding issue of CMOS multigigahertz measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 9, pp. 1813–1823, Sep. 2007.

[18] J. Cha, J. Cha, and S. Lee, "Uncertainty analysis of two-step and three-step methods for deembedding on-wafer RF transistor measurements," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2195–2201, Aug. 2008.

[19] Q. Liang, J. D. Cressler, G. Niu, Y. Lu, G. Freeman, D. C. Ahlgren, R. M. Malladi, K. Newton, and D. L. Harame, "A simple four-port para- sitic de-embedding methodology for high-frequency scattering parameter and noise characterization of SiGe HBTs," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 11, pp. 2165–2174, Nov. 2003.

[20] L. F. Tiemeijer, R. J. Havens, A. B. M. Jansman, and Y. Bouttement, "Comparison of the 'pad-open-short' and 'open-short-load' deembedding techniques for accurate on-wafer RF characterization of high-quality passives," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 723–729, Feb. 2005.

[21] X. Wei, G. Niu, S. L. Sweeney, Q. Liang, X. Wang, and S. S. Taylor, "A general 4-port solution for 110 GHz on-wafer transistor measurements with or without Impedance Standard Substrate (ISS) calibration," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2706–2714, Oct. 2007.

[22] Y. Tretiakov, J. Rascoe, K. Vaed, W. Woods, S. Venkatadri, and T. Zwick, "A new on-wafer de-embedding technique for on-chip RF transmission line

interconnect characterization," in *Proc. ARFTG Conf. Dig.*, Jun. 2004, pp. 69–72.

[23] H.-T. Yen, T.-J Yeh, and S. Liu, "A Physical De-embedding Method for Silicon-based Device Applications," in *PIERS Online*, vol. 5, no. 4, pp. 301–305, 2009.

[24] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[25] J. Song, F. Ling, G. Flynn, W. Blood, and E. Demircan, "A de-embedding technique for interconnects," in *Proc. Elect. Perform. Electron. Packag.*, Cambridge, MA, Oct. 2001, pp. 1371–1375.

[26] M.-H. Cho, G.-W. Huang, K.-M. Chen, and A.-S. Peng, "A novel cascade- based de-embedding method for on-wafer microwave characterization and automatic measurement," in *Proc. IEEE Int. Microw. Symp. Dig.*, Jun. 2004, vol. 2, pp. 1237–1240.

[27] M. H. Cho, C. S. Chiu, G. W. Huang, Y. M. Teng, L. H. Chang, K. M. Chen, and W. L. Chen, "A fully-scalable de-embedding method for on-wafer S-parameter characterization of CMOS RF/microwave devices," in *Proc. IEEE RFIC Symp. Dig.*, Jun. 2005, pp. 303–306.

[28] M.-H. Cho, G.-W. Huang, L.-K. Wu, C.-S. Chiu, Y.-H. Wang, K.-M. Chen, H.-C. Tseng, and T.-L. Hsu, "A shield-based three-port de-embedding method for microwave on-wafer characterization of deep- submicrometer silicon MOSFETs," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2926–2934, Sep. 2005.

[29] J. Song, F. Ling, G. Flynn, W. Blood, and E. Demircan, " A de-embedding technique for interconnects," in *Proc. Elect. Performance Electron. Packag.*, Cambridge, MA, Oct. 2001, pp. 129–132.

[30] A. Issaoun, Y. Z. Xiong, J. Shi, J. Brinkhoff, and F. Lin, "On the deembedding Issue of CMOS multigigahertz measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 9, pp. 1813–1823, Sep. 2007.

[31] M. Y. Bohsali "Millimeter-wave CMOS Power Amplifiers Design," Ph.D. dissertation, EECS., UCB., Berkeley., CA, 2009.

[32] B. Cetinoneri "Advanced CMOS circuits for microwave and millimeter-wave communications," Ph.D. dissertation, Department of Electrical and Computer Engineering, University of California, San Diego, USA, 2011.

[33] W.R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 15, no. 4, pp. 483, Aug. 1992.

[34] D. Karaca, M. Varonen, D. Parved, A. Vahdati and K. A. I. Halonen , "A de-embedding technique for accurate characterization at millimeter-wave frequencies," (to be submitted)

[35] *Microwave Office/Analog Office Measurement Catalog*, AWR Co., El Segundo, CA, 2014.

[36] T. S. D. Cheung and J. R. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, May 2006.

[37] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–144, Jan. 2005.

[38] M. Varonen, M. Karkkainen, M. Kantanen, and K. Halonen, "Millimeter-wave integrated circuits in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1991–2002, Sep. 2008.

[39] A. Sayag, D. Ritter, and D. Goren, "Compact modeling and comparative analysis of silicon-chip slow-wave transmission lines with slotted bottom metal ground planes," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 4, pp. 840–847, Apr. 2009.

[40] D. Sandstrom, M. Varonen, M. Karkkainen, and K. A. I. Halonen, "W-band amplifiers achieving +10 dBm saturated output power and 7.5 dB NF," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3043–3409, Dec. 2009.

[41] M. Varonen "Design and Characterization of Monolithic Millimeter-wave Active and Passive Components, Low-Noise and Power Amplifiers, Resistive Mixers, and Radio Front-Ends," Ph.D. dissertation, Department of Micro and Nano Sciences, Aalto U., Espoo, Finland, 2010.

[42] A. M. Niknejad and H. Hashemi, *mm-Wave Silicon Technology 60 GHz and Beyond*, 1st ed., NY: Springer, 2008.

[43] B. Heydari "CMOS Circuits and Devices beyond 100 GHz," Ph.D. dissertation, EECS., UCB., Berkeley., CA, 2008.

[44] C. K. Liang and B. Razavi, "Systematic transistor and inductor modeling for millimeter-wave design," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 450–457, Feb. 2009.

[45] O. Inac, M. Uzunkol, and G. Rebeiz, "45-nm CMOS SOI technology characterization for millimeter-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 6, pp. 1301–1311, Jun. 2014.

[46] M. S. Gupta, "Power gain in feedback amplifiers, a classic revisited," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 5, pp. 864–879, May 1992.

[47] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," in *IEEE Transactions Electron Devices*, vol. 26, no. 7, pp. 1032-1037, July 1979.

[48] S. C. Cripps "Linear RF Amplifier Theory," in *RF Power Amplifiers for Wireless Communications*, 2nd ed., Norwood: Artech House, 2006, pp. 4-5.

[49] K. Wang, M. Jones, S. Nelson "The S-probe-a new, cost-effective, 4-gamma method for evaluating multi-stage amplifier stability," in *Microwave Symp. Dig.*, vol. 2, pp. 829-832, June 1992.

[50] R. Gilmore "Nonlinear Circuit Simulation Techniques," in *Practical RF Circuit Design for Modern Wireless Systems: Active Circuits and Systems*, vol. 2, Norwood: Artech House, 2003, pp. 208-215.

[51] H.T. Friis, "Noise Figures of Radio Receivers," in *Proc. of the IRE*, vol. 32, no. 7, pp. 419-422, July 1944.

[52] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ: Prentice-Hall, 1997.

[53] B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad, "Millimeter-wave devices and circuit blocks up to 104 GHz in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2893–2903, Dec. 2007.

[54] T. Yao, M.Q. Gordon, K.K.W. Tang, K.H.K. Yau, Y. Ming-Ta, P.Schvan, S.P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," in *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044-1057, May 2007.

[55] Y.S. Lin, G.L. Lee, C.C. Wang, and C.C. Chen " 21.1 mW 6.2 dB NF 77-81 GHz CMOS low-noise amplifier with 13.5±0.5 dB S21 and excellent input and output matching for automotive radars," in *IEEE Radio and Wireless Symp.*, pp. 73-75, Jan. 2014.

[56] D. Lu; Y. Hsu; J. Kao; J. Kuo; D. Niu; K. Lin, "A 75.5-to-120.5-GHz, high-gain CMOS low-noise amplifier," in *Proc. IEEE Int. Microw. Symp. Dig.*, Montreal, QC, Canada, pp. 1-3, Jun. 2012.

[57] A. Tomkins, P. Garcia, S.P. Voinigescu, "A Passive W-Band Imaging Receiver in 65-nm Bulk CMOS," in *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1981-1991, Oct. 2010.

[58] M. Khanpour, K.W. Tang, P. Garcia, S.P. Voinigescu "A Wideband W-Band Receiver Front-End in 65-nm CMOS," in *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1717-1730, Aug. 2008.

[59] D. Pepe and D. Zito "32 dB Gain 28 nm Bulk CMOS W-Band LNA," in *IEEE Microw. Compon. Lett.*, vol. 25, no. 1, pp. 55-57, Jan. 2015.

[60] D. Parveg, M. Varonen, M. Kärkkäinen, D. Karaca, A. Vahdati, K. A. I. Halonen, "Wideband Millimeter-Wave Active and Passive Mixers in 28 nm Bulk CMOS Technology," in *Proc. 4th Eur. Microwave Integrated Circuits Conf.*, Paris, France, Sep. 6–13, 2015, (accepted).

[61] D. Parveg, A. Vahdati, M. Varonen, D. Karaca, M. Kärkkäinen, K. A. I. Halonen, "Modeling and Applications of Millimeter-wave Slow-wave Coplanar Coupled Lines in CMOS," in *Proc. 4th Eur. Microwave Integrated Circuits Conf.*, Paris, France, Sep. 6–13, 2015, (accepted).

[62] A. Vahdati, D. Parveg, M. Varonen, M. Kärkkäinen, D. Karaca, K. A. I. Halonen, "A 100-GHz Phase Shifter in 28-nm CMOS SOI," in *Proc. 4th Eur. Microwave Integrated Circuits Conf.*, Paris, France, Sep. 6–13, 2015, (accepted).